A Symmetrical Hybrid Power Flow Controller

by

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Abstract

A novel power flow controller topology, for flexible AC transmission systems (FACTS), is proposed. It consists of a shunt connected controllable source of reactive power, and two series connected voltage–sourced converters – one on each side of the shunt device. The two converters can exchange active power through a common DC circuit.

By controlling the magnitudes and the angles of voltage vectors injected by the converters, the flow of active power through the line and the amounts of reactive power supplied to the sending and receiving segments of the line, can be simultaneously and independently controlled. The control of the shunt device is coordinated with the control of the converters to provide the bulk of the total required reactive power.

Some distinct properties of the proposed topology are readily observed: (a) The required converters and their coupling transformers are of identical ratings due to the inherent symmetry. (b) The reactive power supplied by the shunt device can be varied in steps, permitting simple implementation. Vernier control of the reactive power supplied to the line segments can be achieved using the converters. (c) The freedom to vary magnitude and phase angle of the injected voltages permits increase in the transmitted power at low values of transmission angle without the increase of voltage magnitude at the midpoint of the line. As the transmission angle increases, the role of voltage injection changes from phase angle control to reactive power compensation, thereby enabling full utilization of converter ratings at any value of the transmission angle.
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Author
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To Ruška, Marija, and Petar for their love and understanding...
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Chapter 1

Introduction

The research presented in this thesis relates generally to the control of the flow of power in an alternating current (AC) transmission system. In particular, it relates to a power flow controller and a method for controlling the flow of active and reactive power on an AC transmission line.

1.1 Background

In most cases, electrical energy is not produced where it is consumed, so it is necessary to transmit power from generation centres (large power plants) to load centres (cities or industrial facilities). High voltage transmission systems transport electrical energy from its source to the point of consumption.

To ensure reliability of supply, and because of economic and other factors, it is common practice to interconnect transmission systems in different geographic or geopolitical regions. As a result, transmission systems are typically large and complex electrical circuits consisting of hundreds of generation/consumption nodes and thousands of transmission lines. Controlling the flow of power between the nodes in such complex circuits is a challenging problem. It is further complicated by the need to control the voltage at each node to within a small tolerance of the rated value.

Historically, there have been only limited means for controlling transmission systems. Node voltages were controlled by mechanically switched shunt connected capacitor or in-
ductor banks, and the power flow through individual lines was controlled by changing taps on phase shifting transformers and by cancelling line inductance by switching capacitors in series with the line. The operating life of mechanical switches is inversely proportional to the rate at which switching cycles are performed under load; hence, control of transmission systems was limited to slow sequential reconﬁgurations designed to reach the desired steady state operating point for a given set of conditions. Dynamic control was not possible, and consequently transients initiated by faults, line and generator outages, or by equipment malfunction, were dealt with by operating the system conservatively and by a practice of overdesign. This resulted in considerable underutilization of system capacity.

The advent of power grade thyristors in the early 1970s made it possible to improve classical means for controlling power systems. Thyristors can be described as one–way switches that begin to conduct when a turn–on pulse is sent to their gate. They stop conducting when the current is brought to zero by other means. Thyristors were ﬁrst used as replacements for mechanical switches, alleviating the problem of reduced operating life due to the number of switching cycles. Applications include thyristor switched capacitors and reactors, and thyristor–based phase angle regulators and tap changers.

Over time, owing to the ability of thyristors to delay the turn–on instant, more sophisticated circuit conﬁgurations have emerged [1] which allow continuous variation of compensator parameters, including static VAr compensators (SVCs) which allow continuous control of shunt connected reactance, and thyristor controlled series capacitors (TCSCs). Considerable deployment of static VAr compensators began in the mid–1970s and, to date, they are the most commonly used power system compensator.

A fundamental characteristic of the power industry is that the demand for power rises steadily, while system upgrades are implemented through large and costly projects. Over the years, energy, environmental, right–of–way, and cost problems have delayed the construction of both generation facilities and new transmission lines, so better utilization of existing power systems has become imperative. In the early 1980s, it was recognized that a change was needed in traditional practices in system planning and operation [2].

Concurrently, technological advancements in the semiconductor industry led to the production of a power grade gate turn–off thyristor (GTO). The GTO is functionally similar to
the thyristor, but it can also be turned off by sending a pulse to its gate. The commercial availability of GTOs in the mid-1980s made it possible to construct large voltage-sourced converters (VSCs)[3]. In principle, VSCs are capable of generating multiphase alternating voltage of controlled magnitude and phase. On one side they have switching elements (GTOs), and on the other is some means of voltage support, typically a DC capacitor.

The application of VSCs in the transmission industry became the subject of considerable research effort in the late 1980s and through the 1990s. The “flexible AC transmission system” (FACTS) refers to a concept of power flow control through AC transmission lines using static converters [4]. Examples of converter based FACTS controllers include the advanced static compensator (STATCOM), the series static synchronous compensator (SSSC), the unified power flow controller (UPFC), and the interline power flow controller (IPFC).

1.2 Literature Review

A comprehensive review of all compensators, classical and modern, can be found in [5].

Analyzing the numbers of control degrees of freedom and constraints that have to be satisfied offers useful insight into the capabilities of different FACTS controllers [6]. As explained above, VSCs can generate voltage of controllable magnitude and phase. This means that each VSC offers two independent degrees of freedom. When a converter is interfaced to a transmission line, the two degrees of freedom available for voltage control can be transformed into freedom to control active and reactive power exchanged with the line. While the exchange of reactive power does not impose further limitations, drawing active power in steady state operation requires that the converter be equipped with an energy storage device, which, in most cases, is impractical. Hence, there is a constraint that, in steady state, a converter must not exchange active power with the line.

The STATCOM [7] uses one VSC connected in shunt to the line. With the active power constraint imposed, the control of the STATCOM is reduced to one degree of freedom, which is used to control the amount of reactive power exchanged with the line. Accordingly, a STATCOM is operated as a functional equivalent of an SVC; it provides faster control than an SVC and improved control range.
An SSSC \cite{8} uses a VSC connected in series with the line. In this case, the active power constraint translates into a requirement that the voltage vector injected by the SSSC must at all times be perpendicular to the current vector. This means that an SSSC is equivalent to a controllable series reactance, i.e., an SSSC can be regarded as the functional equivalent of a TCSC. The SSSC offers faster control, and it is inherently neutral to sub-synchronous resonance.

A UPFC \cite{9} is essentially different from previous compensators. It consists of two voltage sourced converters that share a common DC capacitor. One converter is interfaced in series with the line and the other in shunt. The common DC circuit permits unrestricted exchange of active power between the converters so that active power absorbed from the line by one converter can be supplied to the line by the other. As a result, three degrees of freedom are available. The UPFC can be used to control the flow of active and reactive power through the line and to control the amount of reactive power supplied to the line at the point of installation.

In its basic configuration, an IPFC \cite{10} consists of two voltage sourced converters interfaced in series with two independent transmission lines. As in the UPFC configuration, the converters share a common DC circuit that permits the exchange of active power. By injecting appropriate voltages into the lines, an IPFC can redirect the flow of active power from one line to another, while controlling the amount of reactive power. This concept can be extended without difficulty to N lines.

In the past ten years, pilot installations of the most promising FACTS controllers have been built and commissioned in the United States \cite{11, 12, 13, 14, 15, 16, 17, 18, 19, 20}. Figure 1.1 provides some details on these installations.

### 1.3 Motivation

The main impediment in widespread use of all current FACTS controllers is their considerable price. At present, they are well beyond reach of many utilities. Moreover, it is arguable whether improvements in control performance achieved by a STATCOM or SSSC commercially justify the replacement of their thyristor–based counterparts. The core functionality
Figure 1.1: FACTS installations at the transmission level – USA [21] (Reprinted with permission from Robert Schainker, EPRI)
provided by an IPFC can be largely accomplished by individual line control using classical compensators.

A UPFC offers control options substantially different from those of classical compensators. Nonetheless, due to the need for two converters, the investment required for UPFC installation discourages widespread deployment. Moreover, given its topology, the UPFC can make limited or no use of existing compensators, such as an SVC or switched capacitors.

It is therefore worthwhile to seek alternatives to this compensator that would build upon existing equipment and provide control characteristics equivalent of those offered by a UPFC.

1.4 Thesis Objectives and Organization

This thesis proposes a novel power flow controller topology, for flexible AC transmission systems (FACTS).

The proposed topology consists of a shunt connected controllable source of reactive power, and two series connected voltage-sourced converters – one on each side of the shunt device. The two converters can exchange active power through a common DC circuit.

By controlling the magnitudes and the angles of voltage vectors injected by the converters, the flow of active power through the line and the amounts of reactive power supplied to the sending and receiving segments of the line, can be simultaneously and independently controlled. The control of the shunt device is coordinated with the control of the converters to provide the bulk of the total required reactive power.

Since the converters are used along with the passive components the proposed topology can be considered “hybrid” and consequently, the proposed FACTS controller is named the “Hybrid Power Flow Controller” (HPFC).

The research presented in this thesis shows that the HPFC offers control characteristics similar to those of a UPFC. The main advantage of the HPFC is that it can utilize existing equipment, and hence substantial cost savings in the required converter ratings can be realized.

The thesis is organized into eight chapters, each addressing one of the major objectives. Chapter 2 introduces the proposed topology. Conceptual and detailed diagrams of the
typical HPFC application are presented first. Next, the single phase equivalent circuit is shown and discussed. Then, the constraints applicable to the system variables are identified and explained. After that, the most important technical problems, addressed in the following chapters of the thesis, are outlined and discussed. Finally, the framework for the mathematical description of the system is introduced.

Steady state operation of the HPFC is discussed in Chapter 3. Various operating modes of the HPFC are presented first; then, a methodology for solving all feasible steady state operating points is developed. The methodology observes all the constraints identified in Chapter 2.

Based on the results presented in Chapter 3, various capability curves are plotted and discussed in Chapter 4. A comparison of capability curves for the HPFC and the UPFC is also given.

A controller structure suitable for real time control of the HPFC is developed and explained in detail in Chapter 5.

The controller’s performance is verified under various operating conditions using computer simulation. Some results are presented in Chapter 6.

In Chapter 7, a host of equivalent alternative topologies is presented and discussed. One interesting dual topology is also presented.

Conclusions and thesis’ contributions are delineated in Chapter 8. Some directions for future research are also offered.
Chapter 2

Proposed Topology and Preliminary Analysis

2.1 Proposed Topology

A block diagrammatic view of a typical HPFC application is shown in Figure 2.1. The HPFC is installed on a transmission line that connects two electrical areas.

Central to the HPFC’s topology is the static VAr Compensator (SVC) – i.e. the shunt connected variable susceptance. The key advantage of the HPFC over other known FACTS controllers is that it can be used to retrofit existing equipment (SVCs in this topological variant). Therefore, its point of installation will often be dictated by the location of existing equipment, and in general it will be “within” the transmission line, i.e., at some distance from strong voltage buses.

Next, there are two voltage-sourced converters (VSCs) connected to the associated line segments in series by means of coupling transformers. The converters share a common DC circuit, coupling each other’s DC terminals.

By controlling the magnitudes and angles of voltages supplied by the converters, the flow of active power through the line and the amounts of reactive power supplied to the corresponding line segments can be simultaneously and independently controlled. The control of the shunt device is coordinated with the control of converters to supply the bulk of the total required reactive power.
Figure 2.1: Hybrid Power Flow Controller – typical application

A basic comparison of this topology with the topology of the UPFC highlights the important features of the new circuit. In short, the UPFC’s shunt converter is substituted by an (often existing) SVC, while its series converter is split into two “half sized” ones, installed on each side of the shunt device. Consequently, considerable savings in the total required converter ratings can be achieved. Furthermore, the proposed topology gives rise to retrofit applications, as it permits the upgrade of the functionality of the SVC (and, as will be shown, the switched capacitors). Since there is no need to decommission the SVC, the upgrading of its functionality can be done gradually. This means that the incremental addition of converters increase the functionality incrementally; an important advantage over the UPFC, as in its case the SVC has first to be replaced – resulting in the significant upfront cost.
2.2 Detailed Description

An expanded view of the circuit of Figure 2.1 is shown in Figure 2.2 in the form of a single line diagram. Power flow controller 14, is installed on transmission path 15 that connects region 10 with region 12. Each region may be considered an area of electrical power production and/or power consumption. Transmission path 15 between the regions is thereby divided into two segments: segment 16 connecting area 1 to the power flow controller and segment 18 connecting the power flow controller to area 2. Other, parallel, transmission paths, 20, may also exist between the areas.

The current flowing in line segment 16 is denoted $I_S$, and the current in segment 18 $I_R$. The line to neutral voltage at the point of connection of line segment 16 to the power flow controller is labelled $V_1$. Voltage at the point of connection of line segment 18 to the power flow controller is labelled $V_2$. Transmission line segments 16 and 18 both have substantial lengths which are generally unequal.

Power flow controller 14 includes the power circuit of a shunt connected three-phase variable susceptance, 22. The line to neutral voltage at the high voltage terminals of the variable susceptance is $V_M$. The power circuit for variable susceptance includes transformer 24, one or more branches of capacitive susceptance 26 switchable by controllable switches 28, one or more branches of inductive susceptance 30 switchable or controllable by controllable switches 32, and the optional harmonic filter 34. The circuit of the variable susceptance is equivalent to the circuit of a typical static VAr compensator (SVC). Therefore, functional equivalents of an SVC can be employed in its place. Some widely known equivalents of an SVC include a STATCOM, a synchronous condenser, and a mechanically switched capacitor bank.

The power flow controller also includes voltage-sourced converters 36 and 38. The converters are interfaced in series with their associated line segments by way of transformers 40 and 42, respectively. Each of the converters may include multiple six-pulse converters, interconnected by interstage transformers, to form higher order pulse groups. A comprehensive review of voltage-sourced converter concepts can be found in [5]. The converters share a common DC circuit, coupling each other’s DC terminals. Voltage support at the
Figure 2.2: Hybrid Power Flow Controller – detailed topological diagram
DC terminals is provided by a capacitor.

Finally, controller 46 provides control signals required for operation of the variable susceptance and control signals for operation of the converters of the proposed power flow controller. In Figure 2.2 inputs to the controller are divided into three groups. Reference signals are supplied by the system operator and they represent the desired operating points for the line segments. Parameter settings provide information about the system and about ratings of the installed power circuits. Measured values are the signals proportional to locally accessible currents and voltages. These signals are used for closed loop real time control of the power circuits.

2.3 Equivalent Circuit

A simplified single-phase equivalent circuit including the proposed power flow controller, the interconnected electrical regions and the corresponding line segments is shown in Figure 2.3. Electrical region 10 is represented by its line to neutral Thévenin equivalent voltage source $V_S$. Other voltages have analogous meanings. Values of parameters $R_S$ and $X_S$ are
dominated by the parameters of line segment 16, but also include the Thévenin equivalent of the source impedance representing region 10 and the leakage parameters of transformer 40 (Figure 2.2). Values $V_R$, $R_R$ and $X_R$ are analogous representations of region 12 and line segment 18. Indices “S” and “R” identify “sending” and “receiving” end of the line. Voltage labels $V_1$, $V_2$, and $V_M$ reflect voltages illustrated in Figure 2.2. Voltage sources $V_X$ and $V_Y$ represent the high voltage equivalents of voltages generated by converters 36 and 38, respectively. The variable capacitance, labelled $B_M$, represents the controllable shunt connected variable susceptance. The range of values this parameter can assume depends on the installed power components; in general case it can be positive (capacitive), zero, or negative (inductive).

In Figure 2.3, active and reactive powers of converters 36 and 38 and regions 10 and 12 are respectively labelled $P_X$, $Q_X$; $P_Y$, $Q_Y$; $P_S$, $Q_S$; and $P_R$, $Q_R$. The polarities defined in Figure 2.3 will be used in the mathematical description of the system.

### 2.4 State of the Problem

The power flow controller enables transfer of a specified amount of power (e.g. $P_2$) through the controlled transmission line. Of course, transferring the specified amount of active power through the line stipulates that the reactive powers supplied to the sending and receiving segments of the line ($Q_1$ and $Q_2$) are within certain limits. The particular choice of $Q_1$ and $Q_2$ depends on the parameters of the line and on the given system conditions (i.e. magnitudes of $V_S$ and $V_R$ and their relative angle). In general, the reference values for $P_2$, $Q_1$, and $Q_2$ are obtained from a load flow study.

Consequently, the system operator seeks to supply the reference values for: $P_2$, $Q_1$, and $Q_2$. Such choice of reference values offers the following benefits:

- It is a scalar triplet invariant to the choice of coordinate system.
- It is compatible with standard practices in power system operations.
- The controlled variables can be directly measured at the point of installation of the power flow controller. Hence, closed loop control can be performed locally – without the
uncertainties and delays associated with feedback signals’ transfer over large distances.

The problem to be solved is to structure a control system that is capable to achieve closed loop regulation of variables $P_2$, $Q_1$, and $Q_2$ over a wide range of system conditions and under technical constraints. The constraints, and other technical requirements are identified in the next section.

### 2.4.1 Steady State Circuit Equations and Operating Constraints

For clarity, let the circuit losses be neglected:

$$R_S = R_R = 0 \quad (2.1)$$

To generalize the discussion with respect to the point of equipment installation, let $X_L$ and $k$ be defined as:

$$X_L = X_S + X_R \quad (2.2)$$
$$k = \frac{X_S}{X_L} \quad (2.3)$$

Next, let the following phasors be introduced:

$$V_S = V_S \angle \delta \quad (2.4)$$
$$V_R = V_R \angle 0 \quad (2.5)$$
$$V_X = V_X \angle \delta_X \quad (2.6)$$
$$V_Y = V_Y \angle \delta_Y \quad (2.7)$$

The steady state phasor equations of the AC portion of the circuit are:

$$j k X_L I_S + \frac{1}{j B_M} (I_S - I_R) = V_S - V_X$$
$$-\frac{1}{j B_M} (I_S - I_R) + j (1 - k) X_L I_R = -V_R + V_Y \quad (2.8)$$

To maintain fixed charge on $C_{DC}$, i.e., a steady state condition, the converters represented by voltage sources $V_X$, and $V_Y$ have to operate under the “constraint of power balance”:

$$\text{Re} [V_X I_S^*] = \text{Re} [V_Y I_R^*] \quad (2.9)$$
There are several limit conditions that should be imposed on the operation of the circuit. First, there are limits due to the practical converter sizes:

\[ \sqrt{2} |V_X| \leq V_{X\text{max}} \]  
\[ \sqrt{2} |I_S| \leq I_{X\text{max}} \]  
\[ \sqrt{2} |V_Y| \leq V_{Y\text{max}} \]  
\[ \sqrt{2} |I_R| \leq I_{Y\text{max}} \]

Then, voltages at the equipment terminals are to be limited due to the insulation requirements:

\[ \sqrt{2} |V_1| \leq V_{1\text{max}} \]  
\[ \sqrt{2} |V_2| \leq V_{2\text{max}} \]

Lower limits of terminal voltages may also be specified. These limits were not considered in the thesis, nevertheless, the analysis methodology used in the thesis can be easily adapted to include such additional requirements.

Finally the voltage ratings used for the shunt susceptance will stipulate that:

\[ \sqrt{2} |V_M| \leq V_{M\text{max}} \]

The phasor diagram representing one operating point of the line controlled by the HPFC is shown in Figure 2.4. The operating point represents a power flow lower than the “naturally occurring” power flow. Namely, if the two regions were directly interconnected, the “natural” power transfer between \( V_S \) and \( V_R \) would be [22]:

\[ P_0 = 3 \frac{|V_S||V_R|}{X_l} \sin(\delta) \]

where \( \delta \) represents the angle between the two voltages, as marked in Figure 2.4. The power flow controller changes this naturally occurring power transfer. In the case of the operating point shown in Figure 2.4, reduction of power flow is achieved by injecting voltages \( V_X \) and \( V_Y \) to reduce the angular differences between \( V_S \) and \( V_1 \), and \( V_2 \) and \( V_R \), respectively.

However, there in no guarantee that the depicted operating point is a “viable” one. In other words, there is no guarantee that the operating point satisfying Kirchhoff’s laws
applied to the AC portion of the circuit, also satisfies the constraint of power balance (2.9) and the limit conditions (inequalities (2.10)–(2.16)).

The key question therefore is how to determine all viable operating points for the steady state operation of the circuit.

The viable operating points could be obtained using iterative numerical techniques. A traditional approach is to express the desired output quantities (i.e., $P_2$, $Q_1$, and $Q_2$) and variables subject to constraints (i.e., $P_X - P_Y$, $I_S$, $I_R$, $|V_1|$, $|V_2|$, and $|V_M|$) as functions of control variables ($V_X$, $\delta_X$, $V_Y$, $\delta_Y$, $B_M$); and then, to use numerical iterations to achieve the desired solution. It can be observed that five control variables are at disposal to solve a system of four nonlinear equations, (i.e., $P_2 = P_{2\text{ref}}$, $Q_1 = Q_{1\text{ref}}$, $Q_2 = Q_{2\text{ref}}$, and $P_X - P_Y = 0$). The existence of an additional degree of freedom gives rise to a notion of optimization, and qualifies the problem of selecting viable operating points into the class of problems of nonlinear constrained optimization.

2.4.2 The Problem of Choosing the Equipment Ratings and the Definition of Reachable Sets

To justify the investment required for the installation of any power flow controller, it is necessary to assess the benefits, e.g. increased power transfer or improved stability margin relative to the equipment cost. Hence, a methodology is needed that permits system planners
to obtain the optimum ratings of the controller given the desired range of regulation. This requires to specify all possible operating points of the controller, particularly the operating points that are close to the limit(s). Conversely, some applications may require to solve for the achievable range of line regulation given the ratings of the considered power flow controller.

Specifically, for an HPFC of given ratings to be installed within a specified system, it is required to solve all viable operating points. In mathematical terms, it is required to compute a set of all triplets \((P_2, Q_1, Q_2)\), such that the constraint (2.9) and limit conditions (2.10)-(2.16) are met. The union of these sets for all possible system conditions (various values of the pair \((V_S, V_R)\)) will be termed “the reachable sets” of the line controlled by the HPFC.

Iterative numerical techniques which provide one solution at a time do not address this issue since:

- Only a single operating point might be found in each run. There is no mathematical approach to force an iterative method to identify all solutions within the reachable sets, even if unlimited number of runs is assumed.

- The borders of the reachable sets can not be easily extracted.

- The convergence is problem dependent, and can not be guaranteed in the general case. Moreover, additional analysis is required to separate global and local optimums.

- There is no insight into existence of solutions, nor into effects of the limits. For example, if the required reference triplet \((P_{2\text{ref}}, Q_{1\text{ref}}, Q_{2\text{ref}})\) can not be achieved, further analysis is required to determine whether this is due to the limited voltage capacity of converters, or perhaps a consequence of one of the limits.

- Iterative techniques require a different setup for every optimality criterion. For example, minimizing the converter ratings can be the objective in one application. In another, it may be desired to maximize the power flow and minimize the converter ratings. In yet another, it may be required to maximize the power flow while limiting the reactive power to be supplied from the sending end. Each of these scenarios
requires a different setup and a new set of runs to obtain the operating points.

Chapter 3 presents a numerical technique based on geometric concepts, that yields a solution to the reachable sets without iterations. By using the proposed methodology it is possible to sweep the space of all viable operating points. For each point on a grid, a range of viable solutions is found analytically from the boundaries imposed by the limit conditions. Thus, effects of limits are observed directly, and they can be studied individually or collectively, with virtually no penalty in computation time.

Once the reachable sets are known, they can be further processed to address the question of optimality. Finding a subset of “optimal solutions” from the “complete solutions set” is a simple operation. It requires computing the performance factor algebraically, sorting, and discarding the operating points with the inferior performance factor. This approach is used in Chapter 4 to plot various capability curves.

2.4.3 Requirements for the Dynamic Controller

First, it should be recognized that this is a nonlinear control problem. Controlled variables are active and reactive powers $P_2$, $Q_1$, and $Q_2$:

$$P_2 = \text{Re} \left[(V_M + V_Y)I_R^*\right]$$ (2.18)

$$Q_1 = \text{Im} \left[(V_M + V_X)I_S^*\right]$$ (2.19)

$$Q_2 = \text{Im} \left[(V_M + V_Y)I_R^*\right]$$ (2.20)

Each of the controlled variables includes both the products of state variables, and the products of control variables and state variables.

Second, this is a system of variable structure. The equivalent circuit shows that the order of the system depends on the value of $B_M$. This will be discussed in detail in Chapter 5; for now, it suffices to say that when $B_M > 0$ real and imaginary components of $V_M$ are the state variables, while when $B_M < 0$ voltage $V_M$ is a linear combination of other system voltages.

Next, the importance of enforcing the constraint of power balance (2.9) should be discussed. It was explained before that the difference of $P_X$ and $P_Y$ charges $C_{DC}$. It should be
noted that proper operation of converters (their ability to output voltage) depends directly on $V_{DC}$. If $V_{DC}$ is too high, the converters must be blocked to prevent damage to the power electronic switches. If $V_{DC}$ is too low, the converters are not able to output the rated $V_X$ and $V_Y$, and their ability to control the system diminishes.

Finally, to fully utilize installed equipment, the system should be able to operate near the boundary of the reachable sets. Specifically, it is necessary to permit operation near the converters’ current limits (inequalities (2.11) and (2.13)). For this reason, it is advantageous to control the line currents directly, and therefore have the ability to prescribe the permissible overshoot.

A controller structure that addresses all of the above design criteria is proposed in Chapter 5, and its performance is evaluated in Chapter 6.

2.5 Framework for the Mathematical Description of the System

For the study of power system dynamics it is common to consider voltages and currents using a rotating reference frame. A motivation for using the rotating frame of reference comes from the theory of AC machines. Namely, if phase shifted currents of the same frequency are run through the spatially distributed windings of the machine, the resulting magnetomotive force (MMF) in the air gap of the machine creates the rotating magnetic field. Defining a reference frame that rotates at the same speed provides a tool to study interactions of the magnetic field vector with other pertinent vectors in a frame of reference where vectors’ components are constant in steady state. This greatly simplifies the design of real time controllers, as these controllers can now operate on DC quantities, rather than on sinusoidally varying quantities observed in the windings. This thesis deals both with the steady state and the dynamic analysis of the HPFC; so, for reasons of consistency and notational convenience, the rotating reference frame is exclusively used in the remainder of the thesis.
2.5.1 Rotating Frame of Reference – “d–q” frame

The orientation of axes and the direction of rotation are depicted in Figure 2.5.

In Figure 2.5, the following applies [23]:

\[
\mathbf{F}_{dq0} = K_{abcdq0} \mathbf{F}_{abc}
\]  

(2.21)

\(\mathbf{F}\) are vectors of instantaneous values of current or voltage in the corresponding frame, that is, \(\mathbf{F}_{abc}\) represents a column vector of instantaneous values of current or voltage in “abc” frame of reference, and \(\mathbf{F}_{dq0}\) represents a corresponding vector of instantaneous values of current or voltage in the “dq0” frame of reference. Transformation matrix \(K_{abcdq0}\) is given
Figure 2.6: Hybrid Power Flow Controller – example vector diagram in d–q reference frame

by:

\[
K_{abcdq0} = \frac{2}{3} \begin{bmatrix}
\cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{4\pi}{3}\right) \\
\sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{4\pi}{3}\right) \\
\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}}
\end{bmatrix}
\]

(2.22)

In normal operation of power systems, zero sequence components are small and can be neglected in the analysis. Consequently, the three scalar quantities from “abc space” can be reduced to one vector in “dq space” without loss of information, and the behavior of the system can be studied using vector diagrams in the plane.

A vector diagram, in d–q reference frame representing the same operating point as the phasor diagram of Figure 2.4, is shown in Figure 2.6. Subscripts “dq” on all vectors are understood and therefore omitted.

### 2.5.2 Constraints Revisited in d–q Frame of Reference

The differential equation describing the dynamics of \(V_{DC}\) is:

\[
C_{DC} \frac{dV_{DC}}{dt} = \frac{1}{V_{DC}}(P_X - P_Y)
\]

(2.23)

In steady state \(V_{DC}\) remains constant, therefore,

\[
P_X = P_Y
\]

(2.24)
or, differently formulated and after cancellation of the proportionality factor:

\[ \mathbf{\tilde{V}}_X \cdot \mathbf{\tilde{I}}_S = \mathbf{\tilde{V}}_Y \cdot \mathbf{\tilde{I}}_R \]  \hspace{1cm} (2.25)

The product operator in equation (2.25) has the meaning of scalar product in the dq plane.

The operating limit conditions in the d–q frame are:

\[ |\mathbf{\tilde{V}}_X| \leq V_{\text{Xmax}} \]  \hspace{1cm} (2.26)
\[ |\mathbf{\tilde{V}}_Y| \leq V_{\text{Ymax}} \]  \hspace{1cm} (2.27)
\[ |\mathbf{\tilde{I}}_S| \leq I_{\text{Xmax}} \]  \hspace{1cm} (2.28)
\[ |\mathbf{\tilde{I}}_R| \leq I_{\text{Ymax}} \]  \hspace{1cm} (2.29)
\[ |\mathbf{\tilde{V}}_M| \leq V_{\text{Mmax}} \]  \hspace{1cm} (2.30)
\[ |\mathbf{\tilde{V}}_1| \leq V_{\text{1max}} \]  \hspace{1cm} (2.31)
\[ |\mathbf{\tilde{V}}_2| \leq V_{\text{2max}} \]  \hspace{1cm} (2.32)
Chapter 3

Steady State Operation of the HPFC

This chapter starts by providing a geometric interpretation for the condition of power balance (2.25). Based on this interpretation, viable steady state operating points can be found directly in the geometric space of line currents. All losses have to be neglected to enable elegant analysis.

A systematic and intuitive procedure for solving steady state operating points is then formulated. The procedure is based on the geometric interpretation of the condition of power balance. Several vector diagrams obtained by the application of this procedure are then discussed to provide insight into various operating modes of the HPFC.

A procedure for computing the reachable sets of the HPFC is given next. It is based on representing the limit conditions (inequalities (2.26)–(2.32)) in the space of line currents, and on the geometric representation of power balance. Thus, it becomes possible to find viable operating points analytically as subspaces in the geometric space of line currents. The solutions in the current space can then be mapped “back” into the space of control variables ($\bar{V}_X, \bar{V}_Y, B_M$), and “forward” into the space of transmission line powers ($P_2, Q_1, Q_2$).

Finally, a procedure for selecting the unique “optimal” operating point based on the pre-computed reachable sets is presented.
3.1 Geometric Interpretation of Power Balance

The formulation of power balance given by (2.25) is not convenient as it involves both the control ($\mathbf{V}_X$ and $\mathbf{V}_Y$) and the controlled variables ($\mathbf{I}_S$ and $\mathbf{I}_R$). A formulation of the power balance constraint invariant to changes in converter voltages is therefore preferable.

The condition given by equation (2.24) stipulates the constant stored energy in the DC capacitor. Furthermore, total energy stored in the three-phase susceptance is, in steady state, constant. Therefore, if losses are neglected, condition (2.24) may be replaced by the condition $P_1 = P_2$. While improved, this formulation still does not provide the desired invariance as it depends on voltage vectors $\mathbf{V}_1$ and $\mathbf{V}_2$. The final formulation is obtained by recognizing that if line segments 16 and 18 are lossless, $P_S = P_1$ and $P_2 = P_R$. Hence, for a lossless system the condition given by equation (2.24) can be expressed as:

$$P_S = P_R$$  \hspace{1cm} (3.1)

or, as:

$$\mathbf{V}_S \cdot \mathbf{I}_S = \mathbf{V}_R \cdot \mathbf{I}_R$$  \hspace{1cm} (3.2)

It is advantageous to provide a geometric interpretation for this condition. For a given vector $\mathbf{V}_S$, sending end power $P_S$ is proportional to the projection of $\mathbf{I}_S$ onto $\mathbf{V}_S$. Therefore, as depicted in Figure 3.1, current vectors $\mathbf{I}_{S1}$ and $\mathbf{I}_{S2}$ transfer the same sending end power, as would any other current vector that has its tip on the same line perpendicular to $\mathbf{V}_S$. This line may be considered a “constant power line”. Hence, the constant power line gives the loci of solutions for current $\mathbf{I}_S$ that couple specified value of active power $P_S$ from the voltage source $\mathbf{V}_S$. An analogous constant power line representing solutions for $\mathbf{I}_R$ can be constructed perpendicular to voltage vector $\mathbf{V}_R$. The condition of power balance between the converters can hence be expressed as the requirement to seek the solutions for vectors $\mathbf{I}_S$ and $\mathbf{I}_R$ that reside on the specified matching pair of constant power lines. A pair of constant power lines such that $P_S = P_R$ will be called “equal power lines”. 

CHAPTER 3. STEADY STATE OPERATION OF THE HPFC

3.2 Solving Steady State Operating Points

Based on $P_R$, $Q_S$, and $Q_R$

The concept of equal power lines can be used to formulate a direct procedure for solving steady state operating points based on $P_R(=P_S)$, $Q_S$, and $Q_R$.

The procedure is illustrated on a lossless system, and with an assumed point of the HPFC installation midway between regions 10 and 12. In terms of circuit parameters defined in Figure 2.3, these simplifications are:

$$R_S = R_R = 0$$
$$X_S = X_R$$

Figure 3.2(a)–(f) illustrates the steps of the procedure. In Figure 3.2(a) voltage vectors $\bar{V}_S$ and $\bar{V}_R$ are shown. Equal power lines corresponding to the desired power flows $P_S$ and $P_R$ are added in Figure 3.2(b). Next, current vectors $\bar{I}_S$ and $\bar{I}_R$ are chosen so that their tips lie on these equal power lines. There is hence one degree of freedom in choosing the location for each vector. This degree of freedom can be viewed as freedom to select the amount of reactive power supplied from the corresponding line end. Specifying $Q_S$ selects a unique $\bar{I}_S$, and specifying $Q_R$ selects a unique $\bar{I}_R$. One set of current vectors $\bar{I}_S$ and $\bar{I}_R$ and the resulting $\bar{I}_M$ are shown in figure 3.2(c). With $\bar{I}_S$ and $\bar{I}_R$ known, voltages $\bar{V}_1$ and $\bar{V}_2$ are determined from:

$$V_{1d} = V_{sd} - X_S I_{sq}$$
$$V_{1q} = V_{sq} + X_S I_{sd}$$

(3.4)
CHAPTER 3. STEADY STATE OPERATION OF THE HPFC

\[ V_{2d} = V_{Rd} + X_R I_{Rq} \]
\[ V_{2q} = V_{Rq} - X_R I_{Rd} \]  

(3.5)

Expressed in matrix form equations (3.4) and (3.5) are:

\[
\begin{bmatrix}
V_1 \\
V_2
\end{bmatrix} =
\begin{bmatrix}
0 & X_S \\
- X_S & 0
\end{bmatrix}
\begin{bmatrix}
I_S \\
I_R
\end{bmatrix}
\]  

(3.6)

\[
\begin{bmatrix}
V_1 \\
V_2
\end{bmatrix} =
\begin{bmatrix}
0 & X_R \\
- X_R & 0
\end{bmatrix}
\begin{bmatrix}
I_S \\
I_R
\end{bmatrix}
\]  

(3.7)

Corresponding vectors \( \vec{V}_1 \) and \( \vec{V}_2 \) are shown in figure 3.2(d). Next, voltage \( \vec{V}_M \) is determined based on \( I_M \) and the desired \( B_M \) using:

\[ V_{Md} = - \frac{1}{B_M} I_{Mq} \]
\[ V_{Mq} = \frac{1}{B_M} I_{Md} \]  

(3.8)

Expressed in matrix form (3.8) is equivalent to:

\[
\begin{bmatrix}
V_M \\
0
\end{bmatrix} =
\begin{bmatrix}
0 & - \frac{1}{B_M} \\
\frac{1}{B_M} & 0
\end{bmatrix}
\begin{bmatrix}
I_M
\end{bmatrix}
\]  

(3.9)

Resulting voltage \( \vec{V}_M \) is shown in Figure 3.2(e). Finally, \( \vec{V}_X \) and \( \vec{V}_Y \) are determined from:

\[ \vec{V}_X = \vec{V}_1 - \vec{V}_M \]
\[ \vec{V}_Y = \vec{V}_2 - \vec{V}_M \]  

(3.10)

A complete vector diagram is shown in Figure 3.2(f). It can be observed that the choice of \( B_M \) indirectly affects the magnitudes of \( \vec{V}_X \) and \( \vec{V}_Y \), by bringing the tip of \( \vec{V}_M \) closer or farther to the tips of \( \vec{V}_1 \) and \( \vec{V}_2 \).

After the operating point is found, limit conditions (2.26)–(2.32) can be verified by measurements of relevant vector lengths and the solution can be accepted or dismissed based on this test.

This procedure provides a direct and systematic approach to solve the nonlinear system of equations (2.8) and (2.9), but it is not directly inclusive of limits.
Figure 3.2: A procedure for solving viable steady state operating points based on specified $P_R (= P_S)$, $Q_S$, and $Q_R$. 
CHAPTER 3. STEADY STATE OPERATION OF THE HPFC

3.3 Operating Modes of the HPFC

The above procedure can be used to obtain vector diagrams for the HPFC. Some examples are given in Figure 3.3(a)–(e). For consistency with previous figures, the same simplifications have been used.

The vector diagram of Figure 2.6 is repeated in Figure 3.3(a). The diagram in Figure 3.3(b) is constructed using the same values for line currents, but different value for $B_M$. The resulting vector $\vec{V}_M$ is hence of larger magnitude and the corresponding $\vec{V}_X$ and $\vec{V}_Y$ are different. The comparison of the two diagrams provides an illustration that the HPFC can provide vernier control of the line currents even if based on a step-changed value of the shunt susceptance. This makes the HPFC topology suitable for retrofitting switched capacitors.

The HPFC has the ability to independently control the amount of reactive power exchanged with the sending and receiving ends of the line. This is demonstrated in Figure 3.3(c) where $Q_R$ has been reduced, resulting in new voltage vectors $\vec{V}_M$, $\vec{V}_X$, and $\vec{V}_Y$. The locations of vectors corresponding to the operating point of Figure 3.3(a) are shown in dashed lines to help quantify the difference.

A vector diagram corresponding to an increased power flow is shown in Figure 3.3(d). Increases in the magnitudes of currents $\vec{I}_S$ and $\vec{I}_R$ are a result of the increased relative angles between vectors $\vec{V}_S$ and $\vec{V}_1$, and vectors $\vec{V}_2$ and $\vec{V}_R$, respectively.

Finally, a vector diagram illustrating the power flow reversal is shown in Figure 3.3(e). Relative position of vectors $\vec{I}_M$ and $\vec{V}_M$ indicates that $B_M < 0$, i.e., that the shunt susceptance is dominantly inductive.

3.4 A Methodology to Compute the Reachable Sets of the HPFC

Computing the reachable sets requires a procedure that is capable of sweeping through the entire range of viable operating points. In this section one such procedure is presented. It is developed to be uniformly applicable for all possible system conditions, and to allow direct
Figure 3.3: Line controlled by the HPFC – example vector diagrams
implementation in the form of a computer program. These features, however, come at a price – the procedure is not intuitive. Therefore, an overview of the entire section is first provided to help navigate the reader through the steps of the process.

First, an alternative procedure for computing the operating points based on $\bar{V}_M$ and specified $P_R (= P_S)$ is given. The advantages of this procedure over the one presented in section 3.2 are as follows: (i) it can handle the singularity occurring at $B_M = 0$; (ii) it relies on locally measurable variables; (iii) it is suitable for generalization into the “sweep algorithm”.

The sweep algorithm is presented next. It starts by identifying the possible range of values for $\bar{V}_M$ based on the limit conditions (2.26), (2.27), and (2.30). Then, for each value of $\bar{V}_M$ in this range, limit conditions (2.26), (2.28), and (2.31) are used to restrict the choice of $\bar{I}_S$; and limit conditions (2.27), (2.29), and (2.32) to restrict $\bar{I}_R$. Finally, the constraint of power balance ($P_S = P_R$), is combined with KCL at node $\bar{V}_M$ ($\bar{I}_M = \bar{I}_S - \bar{I}_R$) to further restrict the ranges of $\bar{I}_S$ and $\bar{I}_R$ and obtain the net permissible ranges of $\bar{I}_S$ and $\bar{I}_R$.

The steps of the algorithm are first presented using geometric diagrams in order to provide conceptual insight. Then, an example implementation of the algorithm is given using pseudo code.

### 3.4.1 Solving Steady State Operating Points
Based on $\bar{V}_M$ and $P_R$

Steps of the procedure are illustrated in Figure 3.4(a)–(f). The procedure starts by specifying the desired value for voltage $\bar{V}_M$. Figure 3.4(a) shows one value of $\bar{V}_M$ along with the known $\bar{V}_S$ and $\bar{V}_R$. Equal power lines corresponding to the desired power flow are added in Figure 3.4(b). Current $\bar{I}_M$ is uniquely determined from known values of $\bar{V}_M$ and $B_M$, and it is shown in Figure 3.4(c). Next, corresponding solutions for $\bar{I}_S$ and $\bar{I}_R$ are found by translating $\bar{I}_M$ into a new position so that its tip lies on the constant power line perpendicular to $\bar{V}_S$, and its tail on the constant power line perpendicular to $\bar{V}_R$. This translation can be composed from two successive translations as shown in Figure 3.4(d). (The first one translates the vector $\bar{I}_M$ to the position where its tip lies on the line $P_S = \text{const}$. The direction of the first
translation is arbitrary, indicated by a pair of dashed lines. The second translation moves the resulting $\vec{I}_M$ along the line $P_S = \text{const}$, to the position where its tail lies on the line $P_R = \text{const}$.) The tip of the resulting vector $\vec{I}_M$ coincides with the tip of the solution for $\vec{I}_S$, while its tail coincides with the tip of the solution for $\vec{I}_R$, as shown in Figure 3.4(e). Therefore, it can be concluded that specifying $\vec{V}_M$ and $B_M$ indirectly specifies $Q_S$ and $Q_R$, although the correlation is not transparent.

Voltages $\vec{V}_1$ and $\vec{V}_2$, and the resulting $\vec{V}_X$ and $\vec{V}_Y$ are determined analogously to the procedure described in section 3.2. The final vector diagram is shown in Figure 3.4(f).

This procedure can be adapted to directly account for limit conditions (2.26)–(2.32). This adaptation will be introduced in the presentation of the sweep algorithm.

### 3.4.2 The Sweep Algorithm

The procedure illustrated in Figure 3.4(a)–(f) can be generalized to compute the entire set of permissible steady state operating points. The steps of the generalized procedure will be explained through the following example. For given $\vec{V}_S$ and $\vec{V}_R$, known circuit parameters, and specified value for $B_M$; find all pairs of $\vec{I}_S$ and $\vec{I}_R$ that satisfy the constraint (2.24) and limit conditions (2.26) to (2.32), neglecting losses.

First, solve for $\vec{V}_M$ in terms of $\vec{V}_X$ and $\vec{V}_Y$:

$$\vec{V}_M = a(\vec{V}_S - \vec{V}_X) + b(\vec{V}_R - \vec{V}_Y)$$  \hspace{1cm} (3.11)

where:

$$a = \frac{X_R}{X_S + X_R} \frac{1}{1 - B_M \frac{X_S X_R}{X_S + X_R}}$$  \hspace{1cm} (3.12)

and

$$b = \frac{X_S}{X_S + X_R} \frac{1}{1 - B_M \frac{X_S X_R}{X_S + X_R}}$$  \hspace{1cm} (3.13)

It follows from (3.11) and inequalities (2.26) and (2.27), that the range of all possible solutions for $\vec{V}_M$ is bounded by a circle. The center of this circle “$M$” has the coordinates:

$$M_d = a V_{Sd} + b V_{Rd}$$

$$M_q = a V_{Sq} + b V_{Rq}$$  \hspace{1cm} (3.14)
Figure 3.4: A procedure for solving viable steady state operating points based on specified $\vec{V}_M$ and $P_R (= P_S)$
The diameter “$D_M$” is given by:

$$D_M = 2(aV_{X\max} + bV_{Y\max}) \quad (3.15)$$

The circle and the corresponding vectors $\bar{V}_S$ and $\bar{V}_R$ are shown in Figure 3.5(a). The limit on the magnitude of $\bar{V}_M$ (inequality (2.30)) can now be directly applied as shown in Figure 3.5(b). Solutions for $\bar{V}_M$ in the shaded area are to be dismissed as they violate (2.30). The range of $\bar{V}_M$ that is to be further considered is shown in Figure 3.5(c). An arbitrarily fine grid can now be applied to the range of possible solutions for $\bar{V}_M$, and the corresponding solutions for $\bar{I}_S$ and $\bar{I}_R$ can be attempted for each value of $\bar{V}_M$ as follows.

Consider a particular value of $\bar{V}_M$ as shown in Figure 3.6(a). With the values of $\bar{V}_M$ and $\bar{V}_S$ fixed, $\bar{I}_S$ is a function of only $\bar{V}_X$ and it is given by:

$$I_{Sd} = -\frac{1}{X_S}(V_{Sq} - V_{Mq} - V_{Xq})$$
$$I_{Sq} = \frac{1}{X_S}(V_{Sd} - V_{Md} - V_{Xd}) \quad (3.16)$$

It can be deduced, from equations (3.16) and inequality (2.26), that the range of values of $\bar{I}_S$ for varying $\bar{V}_X$ is bounded by a circle as shown in Figure 3.6(b). The center of the circle “$S$” has the coordinates:

$$S_d = -\frac{1}{X_S}(V_{Sq} - V_{Mq})$$
$$S_q = \frac{1}{X_S}(V_{Sd} - V_{Md}) \quad (3.17)$$

and its diameter “$D_S$” is given by:

$$D_S = \frac{2V_{X\max}}{X_S} \quad (3.18)$$

($V_{X\max}$ is typically selected based on the voltage ratings of the installed converter.)

The limit on the magnitude of $\bar{I}_S$ (inequality (2.28)) is added in Figure 3.6(c). It is a circle centered in the origin with the radius equal to $I_{X\max}$. ($I_{X\max}$ is typically selected based on the current rating of the installed converter.)

Using equation (3.6), the limit on the magnitude of $\bar{V}_1$ (inequality (2.31)) can also be represented as a circle in the current space. It is centered at “$C_1$” given by:

$$C_{1d} = -\frac{1}{X_S}V_{Sq}$$
$$C_{1q} = \frac{1}{X_S}V_{Sd} \quad (3.19)$$
Figure 3.5: Procedure for solving the range of all possible $\vec{V}_M$
Figure 3.6: Procedure for solving the ranges of admissible $\mathbf{I}_S$ and $\mathbf{I}_R$, based on specified $\mathbf{V}_M$
and its diameter \(D_1\) is:
\[
D_1 = \frac{2V_{1\text{max}}}{X_S}
\] (3.20)

This circle is added in Figure 3.6(d). A range of permissible values for \(I_S\) that satisfy the
limit conditions (2.26), (2.28), and (2.31) is the set of points obtained by intersecting the
respective individual sets. The resulting set is shown as the shaded area in Figure 3.6(e).

Limit conditions (2.27), (2.29), and (2.32) have analogous geometric representation. The
coordinates of the center and the diameter of the circle representing the limit on the mag-
nitude of \(V_Y\) (inequality (2.27)) are given as:
\[
R_d = -\frac{1}{X_R}(V_{Mq} - V_{Rq})
\]
\[
R_q = \frac{1}{X_R}(V_{Md} - V_{Rd})
\]
\[
D_R = \frac{2V_{Y\text{max}}}{X_R}
\] (3.21)

The representation of the limit on the magnitude of \(I_R\) (inequality (2.29)) is a circle cen-
tered in the origin with the radius equal to \(I_{Y\text{max}}\). The circle representing the limit on the
magnitude of \(V_2\) (inequality (2.32)) is centered at \(C_2\) with the coordinates:
\[
C_{2d} = \frac{1}{X_R}V_{Rq}
\]
\[
C_{2q} = -\frac{1}{X_R}V_{Rd}
\] (3.23)

and its diameter \(D_2\) is given by:
\[
D_2 = \frac{2V_{2\text{max}}}{X_R}
\] (3.24)

The above three circles are shown in Figure 3.6(f). The resulting permissible range for \(I_R\)
is shown in Figure 3.6(g).

The resulting permissible ranges for currents \(I_S\) and \(I_R\) are now to be further analyzed
to extract all solutions satisfying the constraint of power balance for this \(V_M\). This will be
explained with reference to Figure 3.7(a)–(f).

Figure 3.7(a) shows \(V_S\), \(V_R\), and two pairs of equal power lines. Notice that the intersec-
tion points of equal power lines define an axes, labelled \(l_0\), in Figure 3.7(b). The \(l_0\) coordinate
of an intersection point is proportional to the power transfer through the transmission line.
Figure 3.6 (continued)
Figure 3.6 (continued)
Therefore, translating a pair of equal power lines along $l_0$ changes the transmitted power. Figure 3.7(c) depicts: $\bar{V}_S$, $\bar{V}_R$, axis $l_0$, two pairs of equal power lines, and the considered $\bar{V}_M$. Applying the procedure of Figure 3.2 for varying power flow results in the range of solutions for $\bar{I}_S$ and $\bar{I}_R$ corresponding to this $\bar{V}_M$. The solution pairs $(\bar{I}_{S1}, \bar{I}_{R1})$ and $(\bar{I}_{S2}, \bar{I}_{R2})$, corresponding to power transfers $p1$ and $p2$, respectively, are shown in Figure 3.7(c). For a given $\bar{V}_M$, it may be observed that $\bar{I}_S$ is confined to lie on line $l_S$, parallel to axis $l_0$. Similarly, $\bar{I}_R$ is confined to lie on line $l_R$. ($l_S$ and $l_R$ are shown in Figure 3.7(d).)

Permissible regions for currents $\bar{I}_S$ and $\bar{I}_R$ (from Figures 3.6(g) and (e), respectively) are shown together with lines $l_S$ and $l_R$ in Figure 3.7(e). The constraints are now as follows:

i) $\bar{I}_S$ lies on $l_S$. Points further right are associated with higher power flows.

ii) $\bar{I}_S$ lies in its own permissible region.

iii) $\bar{I}_R$ lies on $l_R$. Points further right are associated with higher power flows.

iv) $\bar{I}_R$ lies in its own permissible region.

v) $\bar{I}_S$, $\bar{I}_R$, and $\bar{I}_M$ are constrained by KCL such that $\bar{I}_M = \bar{I}_S - \bar{I}_R$.

Therefore, let points $x_S$ and $y_S$ denote the intersections of line $l_S$ with the boundary for the permissible values of $\bar{I}_S$, and $x_R$ and $y_R$ the analogous points on the line $l_R$. The solution pairs $(\bar{I}_S, \bar{I}_R)$ are found so that $\bar{I}_S$ lies on the segment $x_Sy_S$, $\bar{I}_R$ lies on the segment $x_Ry_R$, and their difference equals $\bar{I}_M$. Hence, for the example shown in Figure 3.7(f), the tip of $\bar{I}_S$ lies on the segment $z_Sy_S$ where $z_S$ is the projection of $x_R$ onto $l_S$ in the direction of $\bar{I}_M$, while matching solutions $\bar{I}_R$ have their tip on the segment $x_Rz_R$, where $z_R$ is the projection $y_S$ of onto $l_R$ in the direction of $\bar{I}_M$. The solution pair $(\bar{I}_S, \bar{I}_R)$ corresponding to $(y_S, z_R)$ results in the maximum power flow achievable for this $\bar{V}_M$. Analogously, the solutions corresponding to $(z_S, x_R)$ result in the minimum power flow under the same conditions. Notice that each pair $(\bar{I}_S, \bar{I}_R)$ from line segments $z_Sy_S$ and $x_Rz_R$ results in a unique solution for a vector pair $(\bar{V}_X, \bar{V}_Y)$, and consequently to a set of unique solutions for $P_S = P_1 = P_2 = P_R$, $Q_1$, and $Q_2$.

Repeating this procedure for all permissible values of $\bar{V}_M$ yields a range of all permissible steady state solutions for the given $\bar{V}_S$ and $\bar{V}_R$, and the specified $B_M$. 

Figure 3.7: Procedure for solving the range of admissible power transfer, based on specified $\bar{V}_M$, and known ranges of admissible $\bar{I}_S$ and $\bar{I}_R$. 
Each $\tilde{V}_M$ results in the two “snippets” in current space represented by $\bar{x}_{S\bar{y}S}$ and $\bar{x}_{R\bar{z}R}$.

Thus, to sweep the reachable sets of the HPFC, it is required to:

i) sweep through all possible variations of a quadruplet ($V_S$, $V_R$, $\delta$, $B_M$),

ii) for each quadruplet define a (two dimensional) grid for $\tilde{V}_M$,

iii) for each value on the “$\tilde{V}_M$ grid”, find and store at least one of the solution snippets, i.e. one of the segments $\bar{x}_{S\bar{y}S}$ or $\bar{x}_{R\bar{z}R}$.

Algorithm 3.1 represents a pseudo code implementation of this procedure. The reachable sets are packaged into a table; each row of the table corresponds to one described solution (one pair of snippets) in the current space.

The reachable sets carry the complete set of solutions for the viable operating range of the transmission line controlled by the HPFC. As such, they have immense value for system planning studies, as they permit comprehensive evaluation of the benefits of the HPFC installation. In the next chapter, reachable sets are used to plot $P$-$\delta$ curves, and other “capability” curves, for a line controlled by the HPFC.

Another, implementation related, application for the reachable sets is in resolving the operator supplied reference values for $(P_2, Q_1, Q_2)$ into a set of variables required by the real time controller. This is discussed in Appendix B.
Algorithm 3.1 Compute and store the reachable sets table

% Define the ranges of values for which to compute the tables:

**Input** : \( V_{S\text{array}}, V_{R\text{array}} \) % define the arrays of voltage magnitudes

**Input** : \( \delta_{\text{array}} \) % define the array for \( \delta \) grid

**Input** : \( B_{M\text{array}} \) % define the array for \( B_M \) grid

Supply the values of circuit parameters \( \rightarrow k, X_L \)

\[
\text{table} \leftarrow \{ \} \quad \% \text{Create an empty table}
\]

**for all** \( V_S \in V_{S\text{array}} \) **do**

**for all** \( V_R \in V_{R\text{array}} \) **do**

**for all** \( \delta \in \delta_{\text{array}} \) **do**

**for all** \( B_M \in B_{M\text{array}} \) **do**

Find the range of all possible \( \tilde{V}_M \) (Figure 3.5(a)–(c))

Grid this range and store the grid \( \rightarrow \tilde{V}_{M\text{array}} \) % the grid is two dimensional

**for all** \( \tilde{V}_M \in \tilde{V}_{M\text{array}} \) **do**

Find lines \( l_S \) and \( l_R \) (Figure 3.7(d))

Intersect \( l_S \) with the permissible region for \( \tilde{I}_S \) (Figure 3.7(e)) \( \rightarrow x_S, y_S \)

Intersect \( l_R \) with the permissible region for \( \tilde{I}_R \) (Figure 3.7(e)) \( \rightarrow x_R, y_R \%

Adjust the endpoints (Figure 3.7(f))

\[
\text{Adjust}(x_S, x_R) \leftrightarrow z_S, x_R
\]

\[
\text{Adjust}(y_S, y_R) \leftrightarrow y_S, z_R
\]

% Store the adjusted values

\( z_S \) and \( y_S \) \( \rightarrow \tilde{I}_{S\text{min}} \) and \( \tilde{I}_{S\text{max}} \)

\( x_R \) and \( z_R \) \( \rightarrow \tilde{I}_{R\text{min}} \) and \( \tilde{I}_{R\text{max}} \)

Compute \( P_{2\text{min}} \) and \( P_{2\text{max}} \) based on \( \tilde{I}_{R\text{min}} \) and \( \tilde{I}_{R\text{max}} \) \( \rightarrow P_{2\text{min}}, P_{2\text{max}} \)

\[
\text{table} \leftarrow \text{AddRow} \left( [V_S, V_R, \delta, B_M, \tilde{V}_M; \tilde{I}_{S\text{min}}, \tilde{I}_{S\text{max}}, \tilde{I}_{R\text{min}}, \tilde{I}_{R\text{max}}, P_{2\text{min}}, P_{2\text{max}}] \right)
\]

**end for**

**end for**

**end for**

**end for**

\[
\text{Return} : \text{table}
\]
Chapter 4

Capability Curves of the HPFC

The procedure for computing the reachable sets, explained in Chapter 3, was implemented in the form of several MATLAB programs custom developed for this purpose. These programs were used to plot various curves pertinent to the line controlled by the HPFC. Studying these curves provides useful insight into performance of the HPFC relative to other FACTS controllers.

It should be apparent from the discussion in previous chapters that limit conditions (2.26)–(2.32) and the value of engaged $B_M$ have significant impact on the steady state operation of the HPFC. The discussion in this chapter addresses these effects first. Then, the influence of the point of installation of the HPFC within the transmission line is evaluated. Next, example P–δ curves of the UPFC are presented and discussed. Finally, a comparative analysis of the P–δ curves for HPFC and UPFC is given.

4.1 Effects of Limit Conditions and $B_M$

An example set of normalized P–δ curves, corresponding to three discrete values of $B_M$, is shown in Figure 4.1. A positive value, zero, and a negative value of $B_M$ were considered. The considered positive (capacitive) value of $B_M$ is four times larger in magnitude than the considered negative (inductive) value. It should be appreciated that such choice of values corresponds to a typical implementation of an SVC where one inductive bank is regulated to provide vernier control of supplied reactive power between the steps of multiple
banks of capacitance. The value of the selected positive $B_M$ is defined implicitly to permit generalized discussion. Namely, the capacitive ratings of an SVC can be uniquely determined by specifying that: when installed at the “electrical center” of the line (i.e., $X_S = X_R$) it is able to maintain 1p.u. voltage at its terminals when $|\bar{V}_S| = 1\text{p.u.}$, $|\bar{V}_R| = 1\text{p.u.}$ and the angle between these vectors is $\delta_{\text{max}}$. This allows the value of $\delta_{\text{max}}$ to be used to specify the SVC’s capacitive ratings. For this analysis let $\delta_{\text{max}} = 60^\circ$.

The voltage rating of the series converters can be arbitrarily selected. The values $V_{\text{Xmax}} = V_{\text{Ymax}} = 0.2\text{p.u.}$ are used in this section. The base for the voltage is the rated line to neutral voltage. Current ratings of the series converter are expressed relative to the current that would flow through an uncompensated line at $|\bar{V}_S| = 1\text{p.u.}$, $|\bar{V}_R| = 1\text{p.u.}$ at the transmission angle $\delta = 90^\circ$.

In Figure 4.1, the HPFC installed in the middle of the line was considered, and only the limits of injected converter voltage, i.e. limit conditions (2.26) and (2.27), were applied in the calculations used to produce the depicted curves. Two curves for each value of $B_M$ can easily be identified. The upper one corresponds to the maximized power flow, and the lower one to the minimized power flow. Therefore, for a given value of $\delta$ any desired power flow between the two extreme curves can be achieved by appropriate control of the converters. Moreover, it is apparent from Figure 4.1 that ranges of power flow reachable for each value of $B_M$ overlap; therefore, at any given value of $\delta$, power flow can be continuously varied between the lowest and highest curve while using only discrete values of shunt susceptance.

Another set of $P-\delta$ curves is shown in Figure 4.2. Labelling of the curves is analogous to Figure 4.1. In Figure 4.2, in addition to limited magnitudes of converter voltages, magnitudes of terminal voltages, and magnitudes of line currents were limited to one per unit. Due to the application of additional limits possible ranges of solutions are visibly restricted. For example at large values of $\delta$, none of the curves have valid solutions. This is due to the fact that even with full voltage capacity of converters applied to oppose the voltage across the line, current will still be above the limit value, and therefore no solution exists. Hence, for $\delta > 125^\circ$ the converters would have to be bypassed, to avoid damage due to over-current.

At lower values of $\delta$ a sharp decline in maximum power flow is visible on most curves.
Figure 4.1: HPFC P–δ curves ($|\vec{V}_x| \leq 0.2\text{p.u.}$ and $|\vec{V}_y| \leq 0.2\text{p.u.}$)
Figure 4.2: HPFC P–δ curves (\(|\bar{V}_X| \leq 0.2\text{p.u.}, \ |\bar{V}_Y| \leq 0.2\text{p.u.}, \ |\bar{V}_1| \leq 1\text{p.u.}, \ |\bar{V}_2| \leq 1\text{p.u.}, \ |I_S| \leq 1\text{p.u.}, \text{ and } |I_R| \leq 1\text{p.u.})
For example, the upper limit curve for $B_M > 0$ declines sharply for $\delta < 65^\circ$. This is due to the application of terminal voltage limits. Specifically, as the value of $\delta$ reduces while $B_M$ is held constant, the reactive power supplied in the middle of the line increases the magnitude of voltage $V_M$. In order to maintain the terminal voltage levels within the limits, voltages injected by the converters must be used to oppose the increase of $|\bar{V}_M|$. Consequently, the amount of converter voltage remaining to be applied towards power flow control is lower and the maximum power flow drops.

An analogous phenomenon is observed on the lower limit curve for $B_M > 0$. In this case the objective is to minimize the power flow; so, since a part of converter voltage capacity is lost on voltage control, minimum feasible power flow raises.

Finally, with the shunt susceptance equal to zero it is not possible to reverse the power flow without increasing the magnitudes of the voltages at equipment terminals above 1 p.u. Hence, the curve representing the minimized power flow for zero shunt susceptance equals to zero at low values of $\delta$.

### 4.2 Effects of Point of Installation and Relative Converter Sizes

In many applications it is not possible to freely choose the point of installation for the power flow compensator. It is therefore important to evaluate the effects a point of installation may have on the capability curves. Recall the factor $k$ (representative of the point of installation) defined by (2.3). In this section an installation of the compensator “at $k = 0.6$” will be considered.

Two question now arise: first, does this point of installation affect the reachable set of the steady state operating points; and second, is it worthwhile to change the relative size of converters to compensate for the point of installation? Intuitively it seems that selecting voltage ratings of the converters to be proportional to their respective line segment lengths may be beneficial. For example, in an installation quantified by $k = 0.6$, one would compare the reachable sets of a symmetrical HPFC ($V_{X_{max}} = V_{Y_{max}} = 0.2$) with the reachable sets of a HPFC with converter voltage ratings adjusted to $V_{X_{max}} = 0.24$ and $V_{Y_{max}} = 0.16$. This
comparison will be illustrated with reference to Figures 4.3 and 4.4.

Consider the symmetrical HPFC first. Figure 4.3 pertains to the following selection of parameters and limits: $k = 0.6$, SVC $(\delta_{\text{max}} = 60^\circ)$, $V_{X\text{max}} = V_{Y\text{max}} = 0.2\text{p.u.}$, $I_{X\text{max}} = I_{Y\text{max}} = 1.2\text{p.u.}$, $V_{1\text{max}} = V_{2\text{max}} = 1\text{p.u.}$. In Figure 4.3(a), a complete set of P-δ curves (one for each discrete value of $B_M$ is shown. In Figure 4.3(b), these curves are combined to maximize (curve 1), or minimize (curve 2) the power flow for each value of δ. For comparison, a power flow of the line compensated by the SVC (curve 3), and the power flow of the uncompensated line (curve 4), are also shown. Moduli of the line currents are shown in figure Figure 4.3(c). Curves 1S and 1R represent the per unit amplitudes of sending and receiving end currents corresponding to the maximized power flow. Curve 1S demonstrates successful application of current limiting at 1.2p.u.. Curves 2S and 2R correspond to minimized power flow. Curve 4 is the per unit amplitude of current corresponding to the uncompensated line. Finally, converter voltage utilization curves are plotted in Figure 4.3(d). Voltage utilization for converter 36 is defined as: $\omega x_{\text{util}} = \frac{|\vec{V}_{\text{Actual}}|}{V_{X\text{max}}}$, and analogously for converter 38. Thus, voltage utilization factors quantify how close to their voltage ratings are the converters actually operated. For example, voltage utilization of one of the converters might remain low throughout the operating range due to the limits applicable to the other converter, or perhaps due to the line limits. For illustration, consider a simple case where voltage utilization remains lower than 0.9 throughout the entire range of δ. The voltage ratings of that converter could then be reduced by 10% without any penalty in overall system performance. Integrating voltage utilization factors over the region of δ of interest can thus be used as a benchmark to evaluate “appropriateness” of the converter voltage ratings for a given application.

Figure 4.4 shows the analogous set of curves for the power flow controller with converter voltage ratings adjusted to $V_{X\text{max}} = 0.24$ and $V_{Y\text{max}} = 0.16$. The comparison of individual curves leads to the conclusion that (for considered point of installation) the performance of the symmetrical HPFC is largely equivalent to the performance of one with adjusted voltage ratings of the converters. Selecting an HPFC with symmetrical converter ratings simplifies equipment design and manufacturing, and consequently results in the more affordable equipment.
Figure 4.3: \( k = 0.6 \), SVC \( (\delta_{\text{max}} = 60^\circ) \), \( V_{X_{\text{max}}} = V_{Y_{\text{max}}} = 0.2\text{p.u.} \), \( I_{X_{\text{max}}} = I_{Y_{\text{max}}} = 1.2\text{p.u.} \), \( V_{1_{\text{max}}} = V_{2_{\text{max}}} = 1\text{p.u.} \).
Figure 4.4: \( k = 0.6 \), SVC (\( \delta_{\text{max}} = 60^\circ \)), \( V_{X_{\text{max}}} = 0.24 \), \( V_{Y_{\text{max}}} = 0.16 \text{p.u.} \), \( I_{X_{\text{max}}} = I_{Y_{\text{max}}} = 1.2 \text{p.u.} \), \( V_{1_{\text{max}}} = V_{2_{\text{max}}} = 1 \text{p.u.} \).
4.3 Comparison of the HPFC with the UPFC

Prior to the work presented in this thesis, there was no systematic method available for computing the reachable sets of a UPFC installed within the transmission line, while respecting equipment and line limits. The formalism developed here for studying the HPFC, namely introduction of equal power lines concept, can be successfully applied to solve the reachable sets of a UPFC. Details of the methodology inclusive of equipment and line limits are presented in Appendix A.

In this section representative capability curves of the line controlled by the UPFC are presented and discussed, and then a comparison of the P-$\delta$ curves for the HPFC and the UPFC is given.

Capability curves of the line controlled by the UPFC are presented in Figure 4.5. The assumed point of installation is characterized by $k = 0.6$. For the system variables and their reference directions identified in Figure A.1, the following ratings and limits apply. In Figure 4.5(a) only the limits of converter sizes are used, that is STATCOM ($\delta_{\text{max}} = 60^\circ$), and $V_{\text{Bmax}} = 0.4\text{p.u.}$ Curves in Figures 4.5(b)–(d) are obtained using the following additional limits: $V_{\text{ETmax}} = V_{\text{BTmax}} = 1\text{p.u.}$, and $I_{\text{Bmax}} = 1.2\text{p.u.}$ Specifically, ratings of the UPFC’s shunt converter (STATCOM) can be defined analogously to the definition of ratings of the SVC, that is by using $\delta_{\text{max}}$. Orientation of the series converter (its installation in the sending or receiving line segment) can be freely selected – orientation in the receiving line segment was considered here. Consequently, the converter current limit (when applied) needs to be imposed only on the magnitude of $I_R$, and it was set at $I_{\text{Bmax}} = 1.2\text{p.u.}$ Limits of voltage magnitudes at the UPFC terminals (when applied) were set at 1.0 p.u.

In Figures 4.5(a) and (b), curve 1 corresponds to the maximized power flow, curve 2 to the minimized power flow, curve 3 to the power flow through the line compensated with the underlying STATCOM, and curve 4 to the power flow through the line without compensation. The Comparison of Figures 4.5(a) and (b) demonstrates that the equipment and line limits have significant effect on the P-$\delta$ curves. Moduli of the line currents are shown in Figure 4.5(c). Curves 1S and 1R represent the per unit amplitudes of sending and receiving end currents, corresponding to the maximized power flow. Curve 1R demonstrates
Figure 4.5: Example capability curves of the UPFC – effects of limits
successful application of current limiting at 1.2pu. At the same time, current $I_S$ is free to assume any value, and its magnitude (labelled $1S$) goes well above 1.2pu at high values of $\delta$. Curves 2S and 2R correspond to the minimized power flow. Curve 4 is the per unit amplitude of current corresponding to the uncompensated line (included for reference).

Finally, utilization curves are plotted in Figure 4.5(d). Converter voltage utilization is used for the series connected converter, and converter current utilization for shunt. Converter current utilization of the shunt converter is defined as: $\epsilon_{\text{util}} = |I_{\text{Actual}}|/I_{\text{Max}}$. It is apparent from the figure that the respective utilizations of the converters in the UPFC vary greatly with $\delta$. Specifically, at low values of $\delta$, current utilization of shunt converter is low and it improves as $\delta$ increases. In contrast, voltage utilization of series converter is high at low values of $\delta$ and it reduces as $\delta$ is increased. Such performance can be expected as at the low values of $\delta$ power transfer is maximized by increasing the relative angle between the sending and receiving end voltages – the role of the series converter. Little reactive power compensation is required, and therefore the current capacity of shunt converter is poorly utilized. At high values of delta, increase in power transfer requires primarily reactive power support and the current utilization of the shunt converter is high. At the same time, current limit of the series converter precludes using its full voltage capacity and consequently its voltage utilization starts to decline. For values of $\delta > 130^\circ$ voltage capacity of series converter is used to limit the current, and its voltage utilization begins to rise again.

Finally, the P-$\delta$ curves of the HPFC (as shown in Figure 4.3(b)) and the P-$\delta$ curves of the UPFC (as shown in Figure 4.5(b)) are compared in Figure 4.6. Curves 1 and 2 correspond to the line controlled by the HPFC to maximize and minimize the power flow, respectively; Curve 3 corresponds to the line compensated by the underlying SVC; Curve 4 corresponds to the power flow on the uncompensated line; Curves 5 and 6 correspond to the line controlled by the UPFC to maximize and minimize the power flow, respectively; and curve 7 corresponds to the power flow on the line compensated by the underlying STATCOM.

The performance of the two devices is nearly equivalent for $\delta \leq 75^\circ$. At values of $\delta > 75^\circ$ the UPFC offers somewhat better performance. This can largely be attributed to the fact that the STATCOM is a device superior to the SVC, as its ability to supply reactive power
Figure 4.6: Comparison of P–δ curves for the HPFC and the UPFC
does not depend on terminal voltage. Comparison of curves 3 and 7 illustrates this difference projected onto power flow. Another factor that contributes to better performance of the UPFC is the fact that it does not need to limit the magnitude of current $I_S$. Nonetheless, this performance gain comes at a substantially higher price, as the UPFC uses a converter in place of an (often existing) SVC or switched capacitor.

In conclusion, this example illustrates that the HPFC offers the performance characteristics similar to those offered by the UPFC. Furthermore, in many cases the HPFC can be built using two identical converter–transformer subassemblies – a significant advantage for practical installations where a spare transformer may be required for redundancy.
Chapter 5

Dynamic Control of the HPFC

Dynamic control of the HPFC is realized in current space. Namely, voltage vectors $\bar{V}_X$ and $\bar{V}_Y$ are used as control variables for closed loop control of currents $I_S$ and $I_R$ to achieve controlled flows of active and reactive power through the respective line segments.

The closed loop control of current is realized in the “d–q” frame of reference. Decoupled d and q–axis current controllers are employed, analogous to [24]. Stabilization of voltage $\bar{V}_M$ is achieved through introduction of an additional control loop. To deal with changes in system structure associated with changes in $B_M$ (as mentioned in section 2.4.3, and discussed in section 5.2) three controllers are used and they are enabled, one at a time, based on the actual value of $B_M$. Power balance between the converters is maintained by introducing a small correction $\Delta I_S$ into the reference value for $I_S$. $\Delta I_S$ is obtained dynamically based on monitoring the voltage on DC capacitors. This is discussed in detail in section 5.2.5. The existence of a “reachable sets table” (computed as described in section 3.4.2) allows the operator of the HPFC to choose the set–points in such a way as to maintain the operating point within the limits of the installed equipment. In the following discussion it will be assumed that this is always the case.

5.1 Overview

High–level organization of the controller and the conceptual signal flows are shown in Figure 5.1. As illustrated, the controller includes the shunt susceptance control block, 66, and
the converter control block, 64. The susceptance control block determines control outputs to be provided to the shunt susceptance, while the converter control block provides outputs to control operation of the voltage–sourced converters. The reference values for \( P_2, Q_1 \) and \( Q_2 \) are supplied by the transmission system operator. Signals representative of these values appropriate for direct use within the controller are denoted: \( p_{2\text{ref}}, q_{1\text{ref}}, \) and \( q_{2\text{ref}} \). These signals are used for table lookup within the reachable set lookup tables block, 62, to determine the reference signals for blocks 64 and 66.

As described in Chapter 3.3 (through comparison of Figures 3.3(a) and (b)), any given “line operating point” corresponds to infinitely many “internal operating points” (i.e. sets of \( \mathbf{v}_X, \mathbf{v}_Y, b_M, \) etc.). The role of the table lookup block is to enable selection of a unique internal operating point that results in preferred optimal utilization of the installed equipment. The converter control block provides the multiplicity of “status signals” to the table lookup block, to facilitate the choice of the relevant entries in the table. The algorithm for table lookup that selects the optimal HPFC operating point based on the pre–computed reachable sets and user defined cost function is described in Appendix B.

The converter control block is responsible for closed loop dynamic control of the voltage–sourced converters. Inputs to this block are: \( p_{2\text{ref}}, q_{2\text{ref}}, v_{M\text{ref}d}, \) and \( v_{M\text{ref}q} \). As detailed with reference to Figure 3.4, a unique internal operating point can be found based on the desired power transfer \( P_2 \) (approximately equal to \( P_R \) or \( P_S \)) and the specified value for \( \mathbf{V}_M \). Therefore, specifying \( q_{2\text{ref}} \) is, strictly speaking, unnecessary. However, using the value for \( q_{2\text{ref}} \) permits simpler internal organization of the converter control block.

The converter control block outputs signals for control of switching elements in the voltage–sourced converters; the signals denoted as “GTO/MCT/IGBT firing pulses”. Appropriately isolated and buffered signals suitable for direct application to the control terminals of the power electronic switches of voltage–sourced converters are commonly referred to as “firing pulses”. Firing pulses directly control the state of the switches in the VSCs, hence they provide the means for direct control of voltages \( \mathbf{V}_X \) and \( \mathbf{V}_Y \).

At present, electronic switches available at the appropriate power level are: Gate Turn–Off Thyristor (GTO), MOS Controlled Thyristor (MCT), and Insulated Gate Bipolar Transistor (IGBT). A particular choice of converter switching components and the overall number
Figure 5.1: High level organization of the controller 46
of switches will be driven by the economic considerations; hence, the properties of the firing pulses, their number, waveforms, and timing, are implementation dependent and will not be further discussed.

Shunt susceptance control block takes a reference signal $b_{Mref}$ and generates the appropriate control signals for the shunt susceptance. Feedback signals representative of $\vec{V}_M$ and $\vec{I}_M$ are used to facilitate the correct timing of the control pulses and to compute the actual value of shunt susceptance $b_M$. Depending on the implementation of the shunt susceptance, the actual susceptance change will occur with a certain delay relative to the reference value supplied by the table lookup block. An accurate value of $b_M$ is used by the converter control block; therefore, the signal of $b_M$ is supplied directly from the shunt susceptance control block to the converter control block.

The signals at the output of the shunt susceptance control block are denoted as “SCR firing pulses” as silicon controlled rectifiers (SCRs) are used for the switching of the variable capacitor bank and control of the inductor bank. Clearly, if alternative switching and control means are used in the power circuit of variable shunt susceptance, appropriate control signals will be generated.

Shunt susceptance control is today regarded as a mature subject. A thorough review of typical SVC construction and its controller implementation can be found in [5]. Therefore, block 66 will not be further discussed here.

A block diagram of the converter control block is shown in Figure 5.2. Interconnections of the blocks are indicated by using signal labels. Labels in lower case letters are used to indicate scaled signals within the controller. Note that some signal labels represent vector quantities, i.e., ordered pairs or triplets of values. The number of short lines crossing the signal path indicates the “order” of each of these signals. Signal paths with no “crossing lines” represent scalar values.

Signal acquisition, conditioning and scaling is done in block 102. The actual measurement technique will vary with implementation.

Scaled and conditioned signals of all incoming values are passed to block 104 where they are transformed into the rotating reference frame. The transformation is done in accordance with equations (2.21) and (2.22). The value for $\theta$ required for the transformation is the
Figure 5.2: Converter Control – internal organization
input to this block; it is shown at the right hand side.

Block 106 generates the signal $\theta$. This block is an integrator that takes the signal of system frequency as its input. The signal of system frequency is derived as a sum of the base value of frequency $f_B$, and the correction $\Delta f$ generated by 102.

Block 108 monitors the DC capacitors. Depending on the size and practical construction of the voltage-sourced converters, DC capacitors will likely be built as multiple banks of capacitors. The signal of total current can, in such case, be derived based on measurements of current in one capacitor bank and then scaled accordingly to represent the whole set.

Steady state voltage estimates of equivalent sending and receiving end voltages are computed in block 110. Inputs to this block are the signals representing values of the terminal voltages and signals representing the currents flowing through the corresponding line segments. It was explained earlier that the estimates of sending and receiving end voltage are used to reduce the bias on integral elements of the PI gains in the current regulators. The accuracy of the estimates is therefore not crucial, as the integrators will suppress the remaining error. Consequently, the design of this block is not critical and will not be given further attention here.

Block 118 is responsible for DC capacitor voltage control. A correction for sending end current reference $\Delta i_{S_{\text{ref}}}$ is computed based on $v_{\text{DC}}$, $i_{\text{DC}}$, and $\bar{v}_{\text{Se}}$. The internal structure of this block will be reviewed in detail.

Line currents reference values are computed in block 112. The internal structure of this block will be reviewed in detail. It should be noticed that this block receives the signals of reference values $p_{2_{\text{ref}}}$, $q_{2_{\text{ref}}}$, and $\bar{v}_{\text{M_{ref}}}$ supplied from the converter control block, and the value of $b_M$ supplied by the susceptance control block. Based on these values and the values of locally measured and estimated variables, current references are computed and passed to the current regulator.

A current regulator 114 performs closed loop current control. It generates the signals $\bar{v}_X$ and $\bar{v}_Y$, proportional to the required voltages $V_X$ and $V_Y$ to provide the required current, as detailed below.

Signals $\bar{v}_X$ and $\bar{v}_Y$ representing the required voltage vectors are first transformed into the stationary frame of reference, and based on the obtained values the appropriate firing pulses
are generated inside block 116. The value of $\theta$ is required to perform the transformation, while the value of $v_{DC}$ is needed to eliminate the effects of DC voltage variations on the converter output voltages.

To summarize, the dynamic control of the proposed power flow controller is realized in the space of line currents. As such, the reference values at the controller level, that is $p_{2\text{ref}}$, $q_{2\text{ref}}$, and $\bar{v}_{M\text{ref}}$, are first transformed into the reference values for currents in the sending and receiving line segments, that is $\bar{i}_{S\text{ref}}$, and $\bar{i}_{R\text{ref}}$. The closed loop current controllers are then employed to force the system currents to become equal to their respective reference values. Other objectives, such as keeping the DC capacitors charged are achieved by appropriately modifying the reference values for currents. It will become apparent through the discussion of the current regulator that active damping of voltage $\bar{V}_M$ may be required under some conditions. This too is achieved by modifying the current references.

5.2 The Controller Structure

The following discussion of the controller blocks is based on the assumption that the dynamics of DC capacitors charging and discharging are considerably slower than the dynamics of currents and voltages in the AC circuit. Therefore, it is possible to assume that the voltage on DC capacitors varies slowly during the AC circuit transients and that its variation can be suppressed by appropriate switching modulation in block 116. The regulator structure for the DC capacitors’ voltage control will be reviewed separately. This assumption enables a structured overall controller design.

It is helpful to start this discussion by identifying the state variables and reviewing their interdependencies. As should be appreciated, the number of state variables depends on the value of $B_M$.

For $B_M > 0$, i.e., for variable shunt susceptance having capacitive susceptance, there are seven state variables. They are: $I_{sd}$, $I_{sq}$, $I_{rd}$, $I_{rq}$, $V_{Md}$, and $V_{Mq}$ in the AC circuit, and $V_{DC}$ in the DC circuit. Voltage vectors $\bar{V}_X$ and $\bar{V}_Y$ are independently adjustable, and the value for $B_M$ can be arbitrarily selected, hence there are five control variables in the system: $V_{Xd}$, $V_{Xq}$, $V_{Yd}$, $V_{Yq}$, and $B_M$. 
For $B_M < 0$, i.e. for variable shunt susceptance having inductive susceptance, voltages $V_{Md}$ and $V_{Mq}$ are the linear combinations of other system voltages, hence the order of the system reduces to five. The number of control variables remains unchanged.

For $B_M = 0$, current vectors $I_S$ and $I_R$ are identical, i.e. $I_S \equiv I_R$. Hence the order of the system reduces to three; state variables are: $I_{Sd}$, $I_{Sq}$, and $V_{DC}$. The number of control variables in this case reduces to four as $B_M = 0$.

This is summarized in Table 5.1.

In each case voltage vectors $V_S$ and $V_R$ can be regarded as slowly varying disturbances, and their values can be estimated based on locally measured variables. Additionally, and according to the prior assumption, the dynamics of DC capacitors are considerably slower than the dynamics of AC circuit; hence, $V_{DC}$ may be regarded as constant.

Furthermore, it is practical to keep the value of $B_M$ constant during AC circuit transients. The value of $B_M$ can either be varied slowly, or changed instantly and then left constant in the following time interval. With this assumption the number of control variables becomes four in each case.

Now, current regulator 114 of control block 64 may be analyzed as three independent current regulators 122, 124, and 126, depending on the value of $B_M$, as shown in Figure 5.3.

<table>
<thead>
<tr>
<th></th>
<th>$B_M &gt; 0$</th>
<th>$B_M = 0$</th>
<th>$B_M &lt; 0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Order of the system</td>
<td>7</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>State variables</td>
<td>$I_{Sd}$, $I_{Sq}$, $I_{Rd}$, $I_{Rq}$, $V_{Md}$, $V_{Mq}$, $V_{DC}$</td>
<td>$I_{Sd} \equiv I_{Rd}$, $I_{Sq} \equiv I_{Rq}$, $V_{DC}$</td>
<td>$I_{Sd}$, $I_{Sq}$, $I_{Rd}$, $I_{Rq}$, $V_{DC}$</td>
</tr>
<tr>
<td>Number of control</td>
<td>5</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>variables</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Control variables</td>
<td>$V_{Xd}$, $V_{Xq}$, $V_{Yd}$, $V_{Yq}$, $B_M$</td>
<td>$V_{Xd}$, $V_{Xq}$, $V_{Yd}$, $V_{Yq}$</td>
<td>$V_{Xd}$, $V_{Xq}$, $V_{Yd}$, $V_{Yq}$</td>
</tr>
</tbody>
</table>

Table 5.1: State and control variables for various values of $B_M$
Output signals from each of these regulators are scalar multiplied by the corresponding enable signal. For example, output signal $\bar{\text{v}}_{X_P}$ representing the desired value for voltage $\bar{V}_X$ when $B_M > 0$, is scalar multiplied by the signal $En_P$ in block 130. The role of block 128 is to generate appropriate enable signals based on the actual value of $b_M$. Hence, output signals $\bar{\text{v}}_X$ and $\bar{\text{v}}_Y$ representing the desired values for $\bar{V}_X$ and $\bar{V}_Y$ can be generated as simple vector sums of the corresponding regulator outputs. The sum functions are realized by blocks 136 and 146 for signals $\bar{\text{v}}_X$ and $\bar{\text{v}}_Y$, respectively.

5.2.1 The Current Regulator for $b_M > 0$

Current regulator 122 (i.e. current regulator 114 for $b_M > 0$) may be reviewed first. It employs decoupled control of $d$ and $q$ components of line currents. The structure is analogous to [24], with some modifications required to handle the dynamics of $\bar{V}_M$. The complete block diagram is shown in Figure 5.4, and the step–by–step procedure for its construction and selection of parameters is discussed below.

Differential equations describing the system shown in Figure 2.3 can be divided into three groups. First, the differential equations describing the dynamics of line segment 18, are:

$$
L_R \frac{dI_{Rd}}{dt} + \omega L_R I_{Rq} + R_R I_{Rd} = V_{Md} + V_{Yd} - V_{Rd}
$$

$$
L_R \frac{dI_{Rq}}{dt} - \omega L_R I_{Rd} + R_R I_{Rq} = V_{Mq} + V_{Yq} - V_{Rq}
$$

Second, the differential equations describing the dynamics of line segment 16, are:

$$
L_S \frac{dI_{Sd}}{dt} + \omega L_S I_{Sq} + R_S I_{Sd} = V_{Sd} - V_{Xd} - V_{Md}
$$

$$
L_S \frac{dI_{Sq}}{dt} - \omega L_S I_{Sd} + R_S I_{Sq} = V_{Sq} + V_{Xq} - V_{Mq}
$$

And third, the differential equations describing the dynamics of positive shunt connected variable susceptance, that is, the dynamics of shunt connected AC capacitors, are:

$$
\frac{B_M}{\omega} \frac{dV_{Md}}{dt} + B_M V_{Mq} = I_{Md} = I_{Sd} - I_{Rd}
$$

$$
\frac{B_M}{\omega} \frac{dV_{Mq}}{dt} - B_M V_{Md} = I_{Mq} = I_{Sq} - I_{Rq}
$$

The three groups of equations (5.1), (5.2) and (5.3) describe a complex dynamical system. State variables within each group are cross–coupled, and there also exist cross–coupling
Figure 5.3: Current regulator – internal organization
between the groups. Notice that \( V_{Md} \) and \( V_{Mq} \) appear on the right hand side of the equations (5.1) and (5.2) while the \( d-q \) components of line currents appear on the right hand side of equations (5.3). Additional complexity arises from the fact that there are only four control variables in the system with six states.

A regulator suitable for closed loop control of \( I_{Rd} \) and \( I_{Rq} \) can be obtained by using voltage components \( V_{Yd} \) and \( V_{Yq} \) to achieve certain closed loop dynamics. Let (5.1) be rewritten into a more common form:

\[
\begin{align*}
L_R \frac{dI_{Rd}}{dt} &= -R_R I_{Rd} - \omega L_R I_{Rq} + V_{Md} + V_{Yd} - V_{Rd} \\
L_R \frac{dI_{Rq}}{dt} &= -\omega L_R I_{Rd} - R_R I_{Rq} + V_{Mq} + V_{Yq} - V_{Rq}
\end{align*}
\]

The block diagram of this dynamical system is shown between the dashed lines “a” and “b” in Figure 5.5(a). To the left of line “a” are the blocks 202 and 204, representing the approximation for the dynamics of the voltage-sourced converter 38 (i.e. the converter outputting \( \bar{V}_Y \)). Specifically, this converter is regarded as an amplifier that takes the signals \( v_{Yd} \) and \( v_{Yq} \), performs the transformation of these signals into the “abc” frame of reference, and outputs the voltages \( V_{Ya} \), \( V_{Yb} \), and \( V_{Yc} \) that correspond to the voltages \( V_{Yd} \) and \( V_{Yq} \) in the “\( d-q \)” space. All this is bundled into just two blocks in order to simplify the block diagram. The factor \( K_{VSC} \) represents the total gain from the signal to the output voltage, while the first order lag characterized by the time constant \( T_{VSC} \) models the converter delays. Similarly, the blocks 206 and 208, located at the right hand side of the line “b”, represent the approximate transfer function of the current measurement system. At the outputs of these blocks are the current feedback signals: \( i_{Rd} \) and \( i_{Rq} \), respectively.

Suppose that the value of \( \bar{V}_Y \) is formed as shown in Figure 5.5(b). The motivation for such a composition is to cancel the unwanted terms on the right hand side of equations (5.4) and introduce new terms that will result in the desired dynamics. This approach is commonly used in control of FACTS devices [24], and in field-oriented control of induction motor drives [25]. The resulting system is shown in Figure 5.5(c). The dynamics in \( d \) and \( q \) axes are now decoupled and hence they can be dealt with independently. Signals \( ERR_d \) and \( ERR_q \) represent the respective errors due to imperfect cancellation of terms. The integral gains embedded in blocks 252 and 254 are located before the point of error insertion; hence,
Figure 5.4: Current regulator for $B_M > 0$ – complete block diagram
Figure 5.5: Current regulator for $B_M > 0$ – signal flow and equivalent transformations of the block diagram
zero steady state error in current control will be achieved in each loop, provided each loop is
stable. Stability analysis of the current controller relative to errors in estimates of parameters
$x^r_R$ and $r^r_R$ is given in Appendix C. The analysis demonstrates that the current regulator
remains stable for a wide range of error.

By suitable selection of PI gains, the speed and damping of closed loop dynamics of
current components $I_{Rd}$ and $I_{Rq}$ can be adjusted to the desired values. If appropriate
combinations of parameters are used, the closed loop transfer functions from the components
of $i_{Rref}$ to the components of $i_R$ can be approximated by the first order lag blocks, as shown
symbolically in Figure 5.5(d).

An analogous rationale can be used to compose a regulator for closed loop control of $i_S$.
Appropriate choice of PI gains (blocks 256 and 258 in Figure 5.4) in this system can warrant
equivalent dynamics of this regulator and the regulator for $i_R$, irrespective of the actual line
segment lengths. Notice that matching time constants of these controllers is not mandatory,
only practical. Resulting simplified transfer functions from the components of $i_{Sref}$ to the
components of $i_S$ are shown in Figure 5.5(e).

It follows from the above discussion that the signals $v_X$ and $v_Y$ are based on the instan-
taneous value of $V_M$. Therefore, as long as the desired values of $V_X$ and $V_Y$ are “within
reach” of the converters, the dynamics of $V_M$ do not affect the dynamics of $i_S$ and $i_R$. The
converse – that the dynamics of $i_S$ and $i_R$ do not affect the dynamics of $V_M$ – is not true.
A block diagram representing the dynamics of $v_M$ according to equations (5.3), and closed
loop dynamics of $i_R$ and $i_S$ according to Figures 5.5(d) and (e), respectively, is shown in Figure 5.6(a). For sake of simplicity, this block diagram is drawn using the signal representing
the physical variables. With reference values $i_S^0$ and $i_R^0$ brought to the inputs of the current
regulators, the expected steady state value of $v_M$ is given by:

$$
\begin{bmatrix}
0 & -1 \\
1 & 0 \\
b_M & \frac{1}{b_M}
\end{bmatrix}
\begin{bmatrix}
i_S^0 \\
i_R^0
\end{bmatrix}
$$

(5.5)

On the other hand, examination of the block diagram shows that there is no damping
in the dynamics of $v_M$; hence, undesirable oscillations of this voltage will occur with every
change of the operating point. This is illustrated in Figure 5.6(b). A trajectory of $v_M$ after
Figure 5.5 (continued)
Figure 5.6: Block diagram and phase portrait of AC capacitors’ voltage dynamics without active damping
an initial condition type disturbance is a circle centered at \( \bar{v}_M^0 \). The tangent vectors shown in the figure represent the derivatives of \( v_{Md} \) and \( v_{Mq} \) according to the block diagram, or equations (5.3).

Introducing damping into this system is equivalent to adding an additional component to the above tangent vectors that are pointed towards \( \bar{v}_M^0 \). A simple way to achieve this is to subtract the phase delayed value of the tangent vector from \( \tilde{i}_{sref} \). The proposed compensation is shown in Figure 5.7(a). The choice of the phase lag and the gain of the transfer function \( G_C(s) \) implemented in blocks 332 and 334 is coordinated with the phase lag already existing in elements 306 and 308, in order to achieve the appropriate overall phase shift. The resulting change in dynamics is illustrated in Figure 5.7(b).

### 5.2.2 The Current Regulator for \( b_M < 0 \)

The current regulator 126 (i.e. current regulator 114 for \( b_M < 0 \)) is reviewed next. Let \( L_M \) be defined as

\[
L_M = -\frac{1}{\omega B_M}
\]

(5.6)

The differential equations describing the system are:

\[
(L_S + L_M) \frac{dI_{Sd}}{dt} - L_M \frac{dI_{Rd}}{dt} = -R_S I_{Sd} - \omega (L_S + L_M) I_{Sq} + \omega L_M I_{Rq} + V_{sd} - V_{Xd}
\]

\[
(L_S + L_M) \frac{dI_{Sq}}{dt} - L_M \frac{dI_{Rq}}{dt} = \omega (L_S + L_M) I_{Sd} - R_S I_{Sq} - \omega L_M I_{Rd} + V_{sq} - V_{Xq}
\]

\[
-L_M \frac{dI_{Sd}}{dt} + (L_R + L_M) \frac{dI_{Rd}}{dt} = \omega L_M I_{Sq} - R_R I_{Rd} - \omega (L_M + L_R) I_{Rq} + V_{yd} - V_{Rd}
\]

\[
-L_M \frac{dI_{Sq}}{dt} + (L_R + L_M) \frac{dI_{Rq}}{dt} = \omega L_M I_{Sd} + \omega (L_M + L_R) I_{Rd} - R_R I_{Rq} + V_{yd} - V_{Rq}
\]

(5.7)

It is apparent that \( \bar{V}_M \) is no longer a state variable and that consequently additional coupling exists between the current terms. Nonetheless, the presence of a control variable on the right hand side of each of the equations permits direct control of all current components. The block diagram of the controller suitable for closed loop current control is shown in Figure 5.8. Constants \( a, b, c, \) and \( d \) are used to resolve the coupling between the state variables. This permits straightforward selection of the PI gains in the blocks 252, 254, 256, and 258. In fact, these blocks are the same blocks used in the current regulator for \( b_M > 0 \).
Figure 5.7: Block diagram and phase portrait of AC capacitors’ voltage dynamics with active damping
5.2.3 The Current Regulator for $b_M = 0$

Finally, the current regulator suitable for $b_M = 0$ should be reviewed. The differential equations describing the system are:

\[
(L_S + L_R) \frac{dI_{sd}}{dt} = -(R_S + R_R)I_{sd} - \omega (L_S + L_R)I_{sq} + V_{sd} - V_{xd} + V_{yd} - V_{rd} \\
(L_S + L_R) \frac{dI_{sq}}{dt} = \omega (L_S + L_R)I_{sd} - (R_S + R_R)I_{sq} + V_{sq} - V_{xq} + V_{yq} - V_{rq}
\]  \hspace{1cm} (5.8)

It is apparent from (5.8) that there are only two state and four control variables. It is also apparent from nature of this system that the d–q components of voltage $\bar{V}_M$ are linear combinations of d–q components of voltages: $\bar{V}_S$, $\bar{V}_R$, $\bar{V}_X$, and $\bar{V}_Y$. Moreover, if losses are neglected, $\bar{V}_M$ becomes a linear combination of the system voltages given by:

\[
\bar{V}_M = \frac{X_R}{X_S + X_R}(\bar{V}_S - \bar{V}_X) + \frac{X_S}{X_S + X_R}(\bar{V}_R - \bar{V}_Y)
\]  \hspace{1cm} (5.9)

Expressions (5.8) and (5.9) can now be considered as a system of four linear equations with four unknowns, where unknowns are the components of vectors $\bar{V}_X$ and $\bar{V}_Y$. Solving $\bar{V}_X$ and $\bar{V}_Y$ based on desired current dynamics and specified value of $\bar{V}_M$, permits independent control of $\bar{V}_M$ while controlling the dynamics of line currents.

Actively controlling $\bar{V}_M$ is useful as it can position this vector in the desired orientation prior to transition into a different mode of operation, i.e., prior to engaging the shunt susceptance. A controller structure suitable for this mode of operation is shown in Figure 5.9.

5.2.4 The Current Reference Computer

As already discussed, the current reference computer (block 112 in Figure 5.2) is responsible for supplying the current references to the current regulator (block 114 in the same figure). In principle, the operation of the current reference computer block is as follows. Signal $\bar{i}_{\text{Ref}}$ is computed based on the inputs $p_{2\text{ref}}$ and $q_{2\text{ref}}$, and the measured value of $\bar{v}_2$. Next, input $\bar{v}_{M\text{ref}}$ is used to compute $\bar{i}_{M\text{ref}}$ based on the known value of $b_M$. Finally, $\bar{i}_{S\text{ref}}$ is obtained as
Figure 5.8: Current regulator for $B_M < 0$ – complete block diagram
Figure 5.9: Current regulator for $B_M = 0$ – complete block diagram
a vector sum of $\tilde{i}_{\text{Rref}}$ and $\tilde{i}_{\text{Mref}}$. This is the conceptual organization. Specific construction, however, has to deal with the variations in structure of the current controllers due to the changes in value of $B_M$, and to provide suitable inputs for correction of current references provided by the DC voltage controller.

A detailed block diagram of the internal structure of the current reference computer is shown in Figure 5.10. A voltage matrix needed to compute $\tilde{i}_{\text{Rref}}$ based on the values of $p_{2\text{ref}}$ and $q_{2\text{ref}}$ is generated as follows. Signals $v_{2d}$ and $v_{2q}$ are low-pass filtered in blocks 362 and 364 and then fed into the matrix composition block 366. This voltage matrix is inverted in block 368, and subsequently the inverse is used to compute $\tilde{i}_{\text{Rref}}$. The time constant of the low-pass filters must be greater than the time constant of the closed loop current controllers to suppress the influence of voltage dynamics on the signals comprising $\tilde{i}_{\text{Rref}}$. The signal of $\tilde{i}_{\text{Mref}}$ is calculated directly based on the signals $v_{\text{Mrefd}}, v_{\text{Mrefq}}$, and $b_M$. The input signal $\Delta \tilde{i}_{\text{Sref}}$ supplied by the DC voltage regulator is used to prepare the signals $\Delta p_{2\text{ref}}$ and $\Delta q_{2\text{ref}}$ (required to modify $p_{2\text{ref}}$ and $q_{2\text{ref}}$ when $b_M = 0$), and added to the signal of $\tilde{i}_{\text{Mref}}$ by way of block 370. Finally, $\tilde{i}_{\text{Sref}}$ is obtained as a vector sum of $\tilde{i}_{\text{Rref}}$ and the modified value of $\tilde{i}_{\text{Mref}}$ (when $b_M \neq 0$) by way of block 372.

It can be deduced based on this discussion that for $b_M \neq 0$ the presence of $\Delta \tilde{i}_{\text{Sref}}$ ultimately results in the steady state error of $\tilde{v}_M$. Analogously, for $b_M = 0$ the presence of $\Delta \tilde{i}_{\text{Sref}}$ results in the steady state error of $p_2$ and $q_2$. Allowing these relatively small inaccuracies permits implementation of a single DC voltage controller which may be used with any of the three current controllers. Expressed in the simplest terms, this approach allows the system to autonomously converge to the operating point near the operating point obtained from the lookup tables.

### 5.2.5 DC Voltage Control

As already discussed, the voltage of the DC capacitors is directly related to the power balance of voltage–sourced converters. The constraint of power balance and its equivalent formulations were discussed in section 3.1. To recapitulate, it was shown that the condition of power balance expressed by $P_X = P_Y$ (equation (2.24)) can, in a lossless system, be replaced by $\mathbf{V}_S \cdot \mathbf{I}_S = \mathbf{V}_R \cdot \mathbf{I}_R$ (equation (3.2)). Next, the graphical interpretation of this
Figure 5.10: Current reference computer – internal organization
equation was introduced, and the following derivation of permissible steady state operating points relied on maintaining the system on the manifold of equal power exchange, that is, on maintaining the current vectors $\bar{I}_S$ and $\bar{I}_R$ on the respective equal power lines.

It is important to emphasize that the above was deduced under the assumption of a lossless system, and that attempting to operate a real system without a strategy to maintain the charge of the DC capacitors would result in a depletion of charge and thus the disablement of the converters. In this section, a strategy for controlling the charge to the DC capacitors will be discussed using already introduced geometric concepts.

A procedure for finding the steady state operating point of a lossless system was presented using Figure 3.4 and explained in the related discussion. In short, the procedure started by assuming that the desired power transfer and $\bar{V}_M$ are known, and based on the known value of $B_M$ a unique solution for the vectors of line currents was found. The tips of the resulting current vectors $\bar{I}_S$ and $\bar{I}_R$ lie on the respective equal power lines. If it is now assumed that closed loop control of current is operational, and that the steady state value of voltage vector is unchanged, the existence of losses will result in a gradual reduction of charge on the DC capacitor. This conclusion follows from the law of conservation of energy for the system of Figure 2.3. Consequently, in order to maintain the constant charge on the DC capacitors it is necessary to alter the power balance between the sending and receiving end of the line. One way to achieve this is to increase $\bar{I}_S$ in the direction of $\bar{V}_S$, while maintaining $\bar{I}_R$ at the original value. Geometric interpretation of this change is shown in Figure 5.11(a).

Control block 118 (shown in Figure 5.2) provides the DC voltage control. The internal structure of this block is shown in Figure 5.11(b). The DC voltage regulator consists of the inner loop that controls $i_{DC}$ using the PI block 382. Output of this PI block is multiplied by the d–q components of the unit vector oriented in the direction of $\bar{V}_{Se}$. Using the estimate instead of the measured value is possible. The only downside of using estimated values is that if the estimate of voltage is incorrect, the resulting change of $\bar{I}_S$ will not be of minimal magnitude; nonetheless, the integral element in 382 will adjust itself to achieve zero error in $i_{DC}$. Outer loop controlling the voltage on the DC capacitors has only the proportional gain element 384. This is sufficient since the plant (DC capacitor) is an integrator. The required incremental change of $\bar{I}_S$ is identified as $\Delta \bar{i}_{Sref}$ in Figure 5.11(b). This signal is used within
Figure 5.11: DC voltage control – conceptual and block diagrammatic implementation
the current reference computer, block 112, as was already explained.

In summary, voltage on the DC capacitors is controlled by altering the power balance between the sending and receiving end of the line. This permits a simple implementation of the DC voltage controller that is essentially decoupled from the current regulators. Consequently, the overall control system is structured and relatively simple to design. Furthermore, such structuring of the DC voltage regulator permits the system to temporarily depart from the manifold of equal power exchange (during transients) and return to it in steady state.

Finally, for completeness it should be appreciated that an initial charge of DC capacitors is required in order for the voltage–sourced converters to operate. This initial charge can be provided by auxiliary circuits of small rating that will be disconnected once the converters are started.
Chapter 6

Simulation Results

The performance of the controller structure proposed in Chapter 5 has been verified using detailed computer simulations. The simulations were done using the software package “PSCAD” [26] (the complete block diagrams of the model are given in Appendix D). In this chapter a selection of representative simulation results is presented and discussed.

6.1 Model Overview

An overview of the studied system is shown in Figure D.1.

A 200km, 230kV transmission line compensated by the HPFC was studied. “Bergeron’s model of the transmission line inclusive of travel time interpolation and reflections” was selected from the PSCAD library. The positive sequence parameters for the line are given in Table 6.1; zero sequence parameters were estimated by PSCAD. This parameter selection is based on the “Steel Single Circuit (SSC)” towers having “J3” geometry, with “ACSR Pheasant” conductor. The data was compiled from the information available at Bonneville Power Administration’s web site. Resistance was subsequently reduced to achieve $X/R = 20$.

The point of HPFC installation was chosen at 120km from the sending end of the line ($k=0.6$). Converters are coupled to the line using single-phase transformers, each rated 40MVA, 2.1/26.5kV, with a leakage reactance of 0.1p.u. Coupling transformers are connected in delta at the converter side, and in series with their respective line conductor on
### Table 6.1: Transmission line parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>24.86(\mu\Omega/m)</td>
</tr>
<tr>
<td>XL</td>
<td>497.2(\mu\Omega/m)</td>
</tr>
<tr>
<td>XC</td>
<td>304.6M(\Omega/m)</td>
</tr>
</tbody>
</table>

Variable shunt susceptance was realized at the voltage level of 13.8kV, using five, twelve pulse, thyristor switched capacitors banks, and one, twelve pulse, thyristor controlled reactor bank. These devices were interfaced to the line using a 300MVA wye/delta–wye connected transformer, with leakage reactances between each pair of windings equal to 0.1p.u. Figure D.6 shows the internal connections of the thyristor controlled reactor bank, and Figure D.7 depicts the construction of the thyristor switched capacitors (identical for all five banks).

The base value for voltage is: \(V_b = 132.8\text{kV}\) (rated line to neutral voltage), and the base value for current \(I_b = 1500\text{A}\) (approximate current capacity of 1272kcmil Pheasant conductor at +30°C). The base value for power is therefore: \(S_b = 3V_bI_b = 597.6\text{MVA}\).

The converters operate from a DC capacitor bank rated 0.5F 3000VDC, as shown in Figure D.5. Base values for DC voltage and current are 1000V and 1000A, respectively.

### 6.2 Dynamic Performance of Current Regulators

The dynamic performance of the current regulator for \(b_M > 0\) is shown in Figure 6.1. Reference values for \(p_{2\text{ref}}, q_{2\text{ref}}\) and d–q components of \(v_{M\text{ref}}\) (labelled P2ref, Q2ref, and VMref, respectively) were changed in a stepwise fashion at \(t = 0.9\text{sec}\). The PI gains in the current regulators were selected to achieve a response time of approximately one quarter of the period of system voltages. It can be observed from the waveforms that this is accomplished successfully. The overshoot in signals representative of measured values of \(P_2\) and \(Q_2\) (labelled P2m and Q2m, respectively) visible in Figures 6.1(a) and (b), is a result of the action of the current regulators. Specifically, an increase in current through the receiving segment.
of the line comes from the transient action (increase in magnitude) of the voltage $\bar{V}_2$. This in turn comes from the transient action of voltage vectors $\bar{V}_X$ and $\bar{V}_Y$ – their respective magnitudes are shown in Figures 6.1(d) (labelled VXmod and VYmod). Consequently P2m and Q2m considerably overshoot their respective reference values. The small overshoots in line current waveforms, Figures 6.1(e)–(h), are a consequence of using a rudimentary estimator of sending and receiving end voltages (the construction of the estimator is shown in Figure D.12). The diagrams were obtained at $\delta = 50^\circ$, with $b_M = 0.35$.

The dynamic performance of the current regulator for $b_M = 0$ is shown in Figure 6.2. This set of diagrams illustrates decoupled action of current regulators from the control of voltage $\bar{V}_M$. The reference value for $p_{2\text{ref}}$ was changed in a stepwise fashion at $t = 0.9$sec. The transients shown in Figure 6.2(a)–(d) show the dynamics of $p_2$, $q_2$, $q_1$, and the magnitudes of $\bar{v}_X$ and $\bar{v}_Y$, respectively. Then, at $t = 1$sec $v_{Mq\text{ref}}$ is changed linearly as shown in Figure 6.2(e). The actual value of $v_{Mq}$ tracks the reference ideally. Moreover, it is apparent that the dynamics of $\bar{v}_M$ make no effect on the dynamics of current – as seen from diagrams of sending end current shown in Figure 6.2(g) and (h). Such performance confirms the expectations based on the discussion in Chapter 5. The diagrams were obtained at $\delta = 50^\circ$.

The dynamic performance of the current regulator for $b_M < 0$ is shown in Figure 6.3. This time only the value for $p_{2\text{ref}}$ was changed (reduced) at $t = 0.9$sec. The transients shown in Figure 6.3(a)–(h) are analogous to the ones pertinent to $b_M > 0$. The AC ripple visible on the waveforms of reactive power comes from the harmonic current injection of the thyristor controlled reactor. The diagrams of Figure 6.3 were obtained at $\delta = 50^\circ$, with $b_M = -0.1$.

Continued...
CHAPTER 6. SIMULATION RESULTS

Figure 6.1: Dynamic performance of current regulator \( b_M = 0.35 \) - step change of \( p_{2ref} \) and \( q_{2ref} \) coordinated with a change of \( \nu_{Mref} \) at \( t = 0.9s \)
Figure 6.2: Dynamic performance of current regulator \((b_M = 0)\) – step change of \(p_{2ref}\) at \(t = 0.9s\), and linear change of \(v_{Mqref}\) for \(t \in (1s, 1.05s)\)
Figure 6.3: Dynamic performance of current regulator ($b_M = -0.1$) - step change of $p_{2ref}$ at $t = 0.9s$
6.3 Dynamic Performance of DC Voltage Regulator

The performance of the DC voltage controller is illustrated in Figure 6.4. The conditions equivalent to those of Figure 6.1 were used, only this time applied at $t = 1\text{sec}$. Transients shown in Figures 6.4(a)–(d) are therefore equivalent to those of the previous figure, now shown over a longer period of time. Dynamics of voltage $\bar{V}_M$ are shown in Figure 6.4(e) and (f). As discussed in Chapter 5, there is a steady state error in voltage $\bar{V}_M$, due to the independent action of the DC voltage controller. Furthermore, coupling of dynamics of $I_{DC}$ (shown in Figure 6.4(g)) with dynamics of $\bar{V}_M$ are visible. Nonetheless, resulting oscillations are adequately damped. Corresponding dynamics of $I_{DC}$ are shown in Figure 6.4(h). Correlation of dynamics between $I_{dc}$ and $V_{DC}$ is apparent. Moreover, it is apparent that the dynamics of the DC voltage regulator are considerably slower than the dynamics of the current regulators.

For these graphs changes of reference inputs in a stepwise fashion were used. In real applications, however, it can be expected that the reference values will be changed gradually using “ramps” of limited slope. Under such conditions the transient peaks of state variables will reduce in magnitude and fewer oscillations will be initiated. The transients shown in Figure 6.5 illustrate the validity of this discussion. The dynamics shown in Figure 6.5 correspond to the same absolute change of reference as the one shown in Figure 6.4, only this time, the change was applied linearly over a time interval of $0.5\text{sec}$. The transient peak of $I_{DC}$ diminishes, and consequently the dynamic behavior of $\bar{V}_M$ improves considerably. In addition, reducing the transient peak of $I_{DC}$ allows further reduction of the DC capacitance ratings.
Figure 6.4: Dynamic performance of DC voltage regulator – step change of $p_{2\text{ref}}$ and $q_{2\text{ref}}$ coordinated with a change of $\mathbf{v}_{\text{Mref}}$ at $t = 1.0\text{s}$; ($b_{\text{M}} = 0.35$)
Figure 6.5: Dynamic performance of DC voltage regulator – linear change of $p_{2\text{ref}}$ and $q_{2\text{ref}}$ coordinated with a change of $v_{M\text{ref}}$ for $t \in (1.0s, 1.5s)$; ($b_M = 0.35$)
Chapter 7

Equivalent Alternative HPFC Topologies

A number of alternative HPFC topologies can be obtained by replacing one or more sub-circuits with their functional equivalents. Several alternative topologies are discussed in this chapter.

First, the shunt connected controllable susceptance can be formed using a synchronous condenser as shown in Figure 7.1(a), or a STATCOM, as shown in Figure 7.1(b).

Next, augmenting energy storage on the DC bus allows the power flow controller to transiently consume or supply active power, by exchanging energy with the storage device. This is illustrated in Figure 7.2(a). Active power exchange may be realized between one or both of the converters and the network. Through active power exchange, the system transient response would be improved. The long term steady state operation would remain unchanged. Net energy exchange between the power flow controller and the system could also be realized. This is depicted in Figure 7.2(b) where a source or sink of power is connected to the DC bus. Modification of the DC voltage control circuit to accommodate dynamic or static energy exchange with the DC link would be required in this configuration.

A power flow controller may easily be implemented using alternative converter technologies. Two other possible configuration are shown in Figure 7.3. Figure 7.3(a) depicts a power flow converter implemented using current-sourced converters. Although voltage controlled sources are replaced with current controlled sources only minor reformulation of an associ-
Figure 7.1: Alternative HPFC topologies based on replacing shunt susceptance with functional equivalents
Figure 7.2: Alternative HPFC topologies based on augmenting energy storage on the DC bus, or permitting energy exchange with an external device.
cialed controller is required to accommodate the current–sourced converters. The overall operating principle remains substantially the same.

Figure 7.3(b) depicts the use of a direct ac–to–ac converter system to provide the two controllable sources of the power flow converter. Again, low–level controls would require modification, however, the overall operating principle is unchanged.

In place of using the described converters to supply the controllable voltage sources of the proposed power flow controller, various electro–mechanical converters could alternatively be used. Two possible configurations that employ machines to generate the controlled sources are illustrated in Figure 7.4. In Figure 7.4(a), synchronous machines supply the controlled voltages. The voltage amplitudes may be regulated through the individual exciter controls. Each synchronous machine is mechanically coupled to a DC machine. DC machine regulation may then be used to transfer a desired amount of active power from one controlled source to the other. Advantageously, the configuration inherently ensures that power balance is met, and therefore, no external power balancing control action is required. Due to the inherent power balance, regulation of the controlled voltage amplitudes, together with the power flow control between the sources, allows full control of the controller. Figure 7.4(b) depicts a similar configuration that employs a reduced number of machines. A doubly fed induction machine is used to replace one synchronous machine, both dc machines, and the electrical tie between the dc machines. Excitation control of the induction machine may be employed to both vary the amplitude of the controlled source and adjust the power flow between sources. Power balance is, again, inherently ensured.

Figure 7.5 represents a multi–terminal power flow controller with N+1 transmission line segments. In an N+1 terminal power flow controller, N active power flows may be independently controlled. Power balance only requires that the sum of all converter powers be substantially zero (less any losses). All N+1 reactive powers flowing in the transmission line segments may also be controlled. Figure 7.5 gives one particular multi–terminal configuration, where there is one sending end network and N receiving end networks. In this case, powers to receiving ends are independently controlled while the converter on the sending end transmission line segment ensures power balance is achieved. Again, reactive power flows in all transmission line segments may be independently controlled. Midpoint capacitor voltage
Figure 7.3: Alternative HPFC topologies based on alternative series converter technologies
Figure 7.4: Alternative HPFC topologies employing electromechanical energy converters
stabilization can be achieved in the same fashion as with the basic power flow controller topology shown in Figure 2.2.

Figure 7.6 illustrates a dual circuit to the power flow controller of Figure 2.2, that can be obtained by wye to delta transformation of the power flow controller’s circuit of Figure 2.2. The controlled sources are now shunt connected current–sourced converters and the central susceptance is transformed into a series connected reactance. As in the original configuration, the requirement for power balance between the converters exists here as well. This variant of an HPFC can be used to improve control of lines compensated by series capacitors. This circuit too has a number of simpler equivalents; using voltage–sourced converters in place of current–sourced converters is one variant.
Figure 7.6: HPFC dual configuration – suitable for retrofitting series capacitors
Chapter 8

Conclusions

8.1 Summary

A new and useful power flow controller topology for the flexible AC transmission system has been proposed and analyzed in this thesis. The proposed topology uses two equally rated voltage-sourced converters to upgrade the functionality of the existing switched capacitors or static VAR compensators. Since static converters are used together with passive devices, the power flow controller can be considered “hybrid” and it is therefore named a “Symmetrical Hybrid Power Flow Controller” (HPFC).

It has been demonstrated, that by using appropriate converter control the functionality of switched capacitors and SVCs can be changed from reactive power support to the generalized power flow control – the functionality commonly associated with the UPFC. The key benefit of the new topology is that it fully utilizes existing equipment and thereby the required ratings of the additional converters are substantially lower than the ratings of the comparable UPFC.

The research presented in this thesis covers all major aspects of the preliminary equipment design.

First, a methodology was developed to determine all permissible steady state operating points of the line controlled by the HPFC. The methodology is inclusive of all limits, that is, it accounts for limits of converter sizes and limits applicable to terminal voltages at the point of equipment installation within the line. The same formalism was then applied to
solve the reachable sets of the UPFC – a problem that remained open for over 10 years.

Obtained solutions were then presented and discussed in detail. It was shown that the equipment and line limits significantly affect the performance curves and must therefore be accounted for in the system planning studies.

Next, a complete structure of the controller suitable for dynamic control of the HPFC has been developed. The controller’s feedback variables are obtained based on the locally measured values. The controller employs a conceptually new strategy to meet the power balance of the converters; the strategy largely based on the equal power lines concept used to solve the steady state operating points. Consequently, during system transients the HPFC is capable to temporarily leave the manifold of equal power exchange and return to it in steady state. A solution for the practical problem of damping the transients on AC capacitors has also been given. The controller’s performance has been verified using detailed PSCAD modelling.

Finally, several equivalent alternative topologies have been presented and discussed. Notably, a dual configuration of the HPFC suitable for retrofitting series capacitors using shunt connected current–sourced converters has been recognized.

8.2 Thesis Contributions

Major contributions of this work are:

- An original and useful power flow controller topology has been introduced. It consists of the shunt connected controllable source of reactive power and two series connected voltage–sourced converters – one on each side of the shunt device. The two converters can exchange active power through a common DC circuit.

- The concept of “equal power lines” enabling the choice of steady state solutions of line current vectors satisfying the constraint of equal power of the converters, has been introduced.

- An algorithm to solve all possible steady state operating points of the line controlled by the HPFC has been formulated. The algorithm (based on the equal power lines
concept) is inclusive of all equipment and line limits, and can be applied for an arbitrary point of equipment installation “within” the transmission line.

- An analogous algorithm has been formulated for the line controlled by the UPFC.

- A controller structure suitable for dynamic control of the HPFC has been developed. The controller structure does not require exact synchronization to the line voltages.

- A new method to control the charge of DC capacitors in the HPFC, based on the application of equal power lines concept has been developed. The method is also applicable to the UPFC.

- A compensator that provides active damping of AC capacitors in the HPFC has been proposed.

- A number of equivalent alternative HPFC topologies have been identified. Notably, machine based equivalents, and a dual topology suitable for retrofitting series capacitors have been recognized.

### 8.3 Future Research

Associated areas that would benefit from further study include:

- A methodology to select the ratings of series converters based on the size of reactive elements forming the shunt susceptance should be developed.

- An algorithm for selecting the minimal size of DC capacitors based on the parameters of the controlled line and the ratings of converters should be formulated.

- A comprehensive comparison study between the HPFC and other FACTS devices should be done.

- The algorithms for calculation of reachable sets should be optimized for speed. Effects of grid size on the accuracy of the interpolated points should also be evaluated.
• Algorithms for efficient computations of the partial reachable set tables covering the range near the actual operating point should be investigated. Once the computational requirements are determined, suitable parallel processing hardware and software should be developed to make these computations feasible in real time.

• In case of line faults the series converters must be bypassed. Algorithms governing transitions in and out of bypass should be formulated.

• Effects of reduced sending or receiving end voltage (e.g. due to distant fault conditions) on the feasibility of maintaining the charge on the DC capacitors should be investigated.

• Algorithms for estimating sending and receiving end voltages (based on known line parameters) suitable for real time implementation should be investigated. Sensitivity of the controller performance relative to the accuracy of estimation algorithms should be evaluated.

• Maximum speed of power flow modulation achievable by the HPFC should be investigated to evaluate its ability to damp the sub–synchronous resonance.

• An ability of the HPFC to balance the line currents should be studied.

• Equivalent alternative HPFC topologies should be investigated. Particularly appealing are: the IM–SM based machine equivalent owing to its inherent ability to tolerate overloads; and, the dual topology based on series connected capacitor and two shunt connected current–sourced converters as there is a considerable installed series capacitor equipment base that could benefit from retrofit applications.
References


Appendix A

A Method to Compute Reachable Sets of the UPFC

A.1 General Statement of the Problem

A schematic diagram of the studied system is shown in Figure A.1. The UPFC is installed at an arbitrary point within the transmission line. Equivalent reactances between the sending end voltage ($\bar{V}_S$) and the input terminal of the UPFC ($\bar{V}_{ET}$), and between the output terminal of the UPFC ($\bar{V}_{BT}$) and the receiving end voltage ($\bar{V}_R$) are denoted $X_S$ and $X_R$, respectively. $X_S$ and $X_R$ include transformer leakage reactances and machine reactances of the system. In addition, $X_R$ also includes the leakage reactance of the UPFC series transformer. In general, $X_S \neq X_R$. The UPFC is represented by a shunt current source ($\bar{I}_E$), and the series voltage source ($\bar{V}_B$). As the model suggests, all losses (line and converters) will be neglected to help maintain the emphasis of the discussion on the analysis.

Figure A.1: Simplified representation of the line controlled by the UPFC
The objective of the analysis is to find all operating points of the system while respecting limits imposed by the ratings of the installed converters, and voltage limits at the equipment terminals. The following limits will be considered:

\[
\begin{align*}
|\vec{V}_B| & \leq V_{B_{\text{max}}} \quad (A.1) \\
|\vec{I}_R| & \leq I_{R_{\text{max}}} \quad (A.2) \\
|\vec{I}_E| & \leq I_{E_{\text{max}}} \quad (A.3) \\
|\vec{V}_{ET}| & \leq V_{ET_{\text{max}}} \quad (A.4) \\
|\vec{V}_{BT}| & \leq V_{BT_{\text{max}}} \quad (A.5)
\end{align*}
\]

Inequalities (A.1) and (A.2) represent the voltage and current limit of the series converter. Inequality (A.3) represents the current limit of the shunt converter. Finally, (A.4) and (A.5) represent the voltage limits on the equipment terminals. Should it be required, lower limits on one or both terminal voltages can also be applied (limit condition (A.4) would then take the form: \( V_{\text{min}} \leq |\vec{V}_{ET}| \leq V_{\text{max}} \)).

Imposing limits on both the shunt current and the UPFC terminal voltage, \( \vec{V}_{ET} \), directly limits the required shunt converter voltage.

The UPFC consists of two converters that share a common DC circuit. If there is no energy storage device coupled to the DC circuit, then, in steady state operation, the active power exchanged between the series converter and the line must be supplied (discharged) by the shunt converter. Equation (A.6) describes this condition.

\[
\text{Re} (\vec{V}_{ET} \cdot \vec{I}_E^*) = \text{Re} (\vec{V}_B \cdot \vec{I}_R^*) \quad (A.6)
\]

This condition introduces nonlinearity to the mathematical model of the UPFC, and adds significant complexity to the problem.

As discussed in section 3.1, in a lossless system the condition of power balance of the converters can be replaced by the requirement to seek \( \vec{I}_S \) and \( \vec{I}_R \) with the tips on the equal power lines. Therefore (A.6) can be replaced by (3.2).
**A.2 Circuit Decomposition**

The circuit of Figure A.1 can be decomposed, based on the principle of superposition, into two circuits shown in Figure A.2. This permits independent analysis of the influence of series and shunt converter on $I_S$ and $I_R$. Comparing Figure A.1 and A.2 it can be deduced:

$$I_S = I_A + \Delta I_S \quad (A.7)$$
$$I_R = I_A - \Delta I_R \quad (A.8)$$

Expressions for current components of (A.7) and (A.8) are:

$$I_A = \frac{\bar{V}_S - \bar{V}_R}{jX_L} + \frac{\bar{V}_B}{jX_L} \quad (A.9)$$
$$\Delta I_S = (1 - k)I_E \quad (A.10)$$
$$\Delta I_R = kI_E \quad (A.11)$$

where $X_L$ and $k$ are defined by (2.2) and (2.3), respectively. Furthermore, $I_A$ is composed of $I_0$ and $I_B$, defined as:

$$I_0 = \frac{\bar{V}_S - \bar{V}_R}{jX_L} \quad (A.12)$$
$$I_B = \frac{\bar{V}_B}{jX_L} \quad (A.13)$$
The composition of $\bar{I}_A$ is shown in Figure A.3. $\bar{I}_A$ resides within the circle centered at $\bar{I}_0$ and with a radius specified by the voltage limit of the series converter, as per (A.13). This circle will be called the “$\bar{I}_A$ circle”. $\bar{I}_A$ circle gives a graphical interpretation to inequality (A.1).

According to (A.10) and (A.11) $\Delta \bar{I}_S$ and $\Delta \bar{I}_R$ are co-linear, and their sum is equal to $\bar{I}_E$. However, $\bar{I}_E$ is also the difference between $\bar{I}_S$ and $\bar{I}_R$, as shown in Figure A.4. Hence, the solution pair $(\bar{I}_S, \bar{I}_R)$ can be viewed as a special composition of $\bar{I}_A$ and $\bar{I}_E$, where the tip of $\bar{I}_A$ lies on $\bar{I}_E$. This “point of contact” is denoted as “$x$” in Figure A.4. Location of point “$x$” on $\bar{I}_E$ is uniquely determined by the factor $k$.

The relation of Figure A.4 therefore imposes an additional constraint on $\bar{I}_A$. As determined in the previous section, power balance stipulates that $\bar{I}_S$ and $\bar{I}_R$ lie on the equal power lines. Thus, for a given power transfer $p_1$ the tip of $\bar{I}_E$ must lie on the constant power line $P_S = p_1$, and its tail on the line $P_R = p_1$. For a given amplitude of $\bar{I}_E$, a family of possible solutions for $\bar{I}_E$ exists, as shown in Figure A.5. The tip of each associated $\bar{I}_A$ vector must lie at point “$x$” on the $\bar{I}_E$ vector. These points are marked by dots on $\bar{I}_E$ vectors. The locus of all possible $\bar{I}_A$ vectors (corresponding to the given power transfer $p_1$, and a given amplitude of the vector $\bar{I}_E$) is an ellipse as shown in Figure A.5.

Power balance therefore requires the tip of $\bar{I}_A$ to lie on an ellipse. If the orientation of $d$–axis is aligned with $\bar{I}_0$, then the power transfer $p_1$ determines the $d$ coordinate of the ellipse’s center, but it does not change its shape and orientation. The ellipse that corresponds to $p_1 = 0$ can be described by the parametric equation:
Figure A.4: Vectorial composition of $\mathbf{I}_S$ and $\mathbf{I}_R$

Figure A.5: Family of solutions for $\mathbf{I}_E$ and $\mathbf{I}_A$

\[
\begin{bmatrix}
  x_d \\
  x_q
\end{bmatrix} = \mathbf{R}(\theta) \cdot |\mathbf{I}_E| \cdot \begin{bmatrix}
  a & 0 \\
  0 & b
\end{bmatrix} \cdot \begin{bmatrix}
  \cos(\zeta) \\
  \sin(\zeta)
\end{bmatrix}
\]  
(A.14)

where “\(\zeta\)” is the parameter taking values in the set: \([0, 2\pi]\) and \(\mathbf{R}(\theta)\) is the rotation matrix defined as:

\[
\mathbf{R}(\theta) = \begin{bmatrix}
  \cos(\theta) & -\sin(\theta) \\
  \sin(\theta) & \cos(\theta)
\end{bmatrix}
\]  
(A.15)

The angle \(\theta\) is defined as:

\[
\theta = \delta_R + \alpha - \pi/2
\]  
(A.16)

where \(\delta_R\) is the angle between \(\mathbf{V}_R\) and the d–axis, and \(\alpha\) is given by (A.17).

\[
\tan(2\alpha) = \frac{k \sin(2\delta)}{1 - 2k \sin^2(\delta)}
\]  
(A.17)

The quadrant of the solution is determined from:

\[
\text{sign}(\sin(2\alpha)) = \text{sign}(\cos(\delta))
\]  
(A.18)
Lengths of major and minor axis are given as:
\[
a = c + d \quad \text{(A.19)} \\
b = c - d \quad \text{(A.20)}
\]

Constants \(c\) and \(d\) are:
\[
c = \frac{1}{2 \sin(\delta)} \quad \text{(A.21)} \\
d = \frac{1}{2} \sqrt{-\frac{1}{\sin(\delta)^2} - 4k(1 - k)} \quad \text{(A.22)}
\]

where \(\delta\) is the angle between \(\hat{V}_S\) and \(\hat{V}_R\).

An operating region can exist, if and only if the circle constraint on \(\hat{I}_A\) as well as the ellipse constraint on \(\hat{I}_A\) have a common area.

Note the following important results: (A.1) is satisfied by choosing the appropriate radius of the \(\hat{I}_A\) circle; (A.3) is satisfied by limiting the value of \(|\hat{I}_E|\) used in the ellipse equation; and the condition of power balance is satisfied inherently through definition of the ellipse, that is, by forcing the ends of the vector \(\hat{I}_E\) to reside on equal power lines.

To summarize, the method presented provides a powerful tool to seek the solutions for \(\hat{I}_S\) and \(\hat{I}_R\) that reside on a manifold defined by the condition of equal power exchange between the converters. Hence, the nonlinearity due to (A.6) is eliminated, making a general analysis possible. In the next section this methodology will be used to solve for the operating points associated with the minimum and maximum power flow. A method to impose limit conditions (A.2), (A.4), and (A.5) will also be presented.

### A.3 Minimum and maximum power flow

Changing the transmitted power through the line corresponds to translating the point of intersection of equal power lines along the \(d\)–axis. This results in translation of the ellipse circumscribed by point “\(x\)” on \(\hat{I}_E\). Any valid solution pair \((\hat{I}_S, \hat{I}_R)\) requires the tip of \(\hat{I}_A\) to coincide with point “\(x\)” on \(\hat{I}_E\). Maximum power flow is therefore obtained when the ellipse is translated in positive direction until it is tangent to the \(\hat{I}_A\) circle. Conversely, the minimum power flow is realized when the ellipse is translated in negative direction until it is tangent to
APPENDIX A. A METHOD TO COMPUTE REACHABLE SETS OF THE UPFC

Figure A.6: Geometric interpretation of the minimum and maximum power flow

the $\mathbf{I}_A$ circle from the other side. These two conditions are graphically shown in Figure A.6.

A.4 Additional limits

It was stated that solution pairs obtained using the proposed process only meet power balance and limit conditions (A.1) and (A.3). Nonetheless, remaining limit conditions can be imposed as follows.

Currents $\mathbf{I}_S$ and $\mathbf{I}_R$ can be expressed as:

\[
\mathbf{I}_S = \frac{\mathbf{V}_S}{j k X_L} - \frac{\mathbf{V}_{ET}}{j k X_L} \tag{A.23}
\]

\[
\mathbf{I}_R = -\frac{\mathbf{V}_R}{j (1 - k) X_L} + \frac{\mathbf{V}_{BT}}{j (1 - k) X_L} \tag{A.24}
\]

Examination of these expressions reveals that the limits specified by (A.4) and (A.5) can be represented as circles in the current space, as depicted in Figure A.7. The first terms in (A.23) and (A.24) define the location of the circle centers, while the limit conditions (A.4) and (A.5) define their radii. $\mathbf{I}_S$ is therefore constrained to lie within the $V_{ET \text{max}}$ circle marked in Figure A.7, while $\mathbf{I}_R$ is constrained to lie within the $V_{BT \text{max}}$ circle. Finally, the series converter current limit is represented by a circle centered at the origin with radius $I_{B \text{max}}$. For the UPFC orientation shown in Figure A.1, it is the receiving end current, $\mathbf{I}_R$, that must lie within the $I_{B \text{max}}$ circle. These additional constraints may indirectly limit the magnitude of $\mathbf{V}_B$ to some value less than $V_{B \text{max}}$, and the magnitude of $\mathbf{I}_E$ to some value less than $I_{E \text{max}}$. 
Application of these limits will be illustrated through the following example: Suppose that $\bar{V}_S$, $\bar{V}_R$, circuit parameters, equipment limits, and line limits are given. Take a specific value of $\bar{I}_E$ such that $|\bar{I}_E| \in [0, I_{Emax}]$. Solve for all possible steady state operating points of the UPFC under these conditions.

The solution for this problem is explained based on Figure A.8. Figure A.8 is an extension of Figure A.7; therefore, only the additional elements will be discussed. In Figure A.8, an ellipse that corresponds to zero power transfer and a given amplitude $|\bar{I}_E|$ is shown centered at the origin of the $d$–$q$ coordinate system. Along with it are shown the equal power lines, and the specific $\bar{I}_E$ that is being considered. The $\bar{I}_A$ circle is also shown.

Changing the transmitted power results in translation of the ellipse. Specifically, this results in the translation of $\bar{I}_E$, and its associated point “$x$”. Corresponding trajectory of “$x$” is a straight line – shown dashed in Figure A.8. This line intersects with the $\bar{I}_A$ circle at points “$y$” and “$z$”. Power balance stipulates that the tip of $\bar{I}_A$ contacts $\bar{I}_E$ at “$x$”; hence, the tip of $\bar{I}_A$ lies on line segment $yz$. Limit conditions discussed in this section require that $\bar{I}_S$ and $\bar{I}_R$ lie within their respective limit circles. Based on Figure A.4, the tip of $\bar{I}_S$ coincides with the tip of $\bar{I}_E$, while the tip of $\bar{I}_R$ coincides with the tail of $\bar{I}_E$. Therefore, the tip of $\bar{I}_E$ must lie within the circle labelled: $V_{ETmax}$, and its tail within the circles labelled: $V_{BTmax}$ and $I_{Bmax}$. In Figure A.8, “$p$” is the point on $yz$ farthest to the right that still respects the current limit. Hence it yields the solution associated with the maximum power flow for the given point “$x$”. Point “$y$” is associated with the minimum power flow.

This example illustrates that application of $V_{ETmax}$, $V_{BTmax}$, and $I_{Bmax}$ limits may result
in restricting the admissible set of solutions for UPFC operating points into a subset of solutions obtained based on applying only the $I_{E_{\text{max}}}$, and $V_{B_{\text{max}}}$, limits.

Other limits can be arbitrarily applied. For example, reactive power supplied by the sending end can be limited; the border of this limit would be represented by a line parallel to $V_S$. Evaluating effects of the orientation of the series converter is also straightforward. If the series converter is installed in the line segment connected to the sending end, it would suffice to apply the current limit to $I_S$, instead of to $I_R$, as was the case here.

The methodology shown in this example can be generalized to solve for all possible operating points of the UPFC. First, the process would be repeated for every $I_E$ of the given amplitude, that is, for every point of the ellipse. Next, this would be repeated for all $|I_E| \in [0, I_{E_{\text{max}}}]$. Union of all obtained solutions would represent the set of all permissible solutions for the UPFC operating points.

Once all permissible operating points are deduced, those associated with the minimum and maximum power flow are identified. The procedure can be repeated for all values of sending and receiving end voltages, i.e., any angle $\delta$ between the two voltages, and P–$\delta$ curves and other pertinent curves for a line controlled by a UPFC can be plotted.
Appendix B

Reachable Sets Table Lookup for Application in the Controller

As discussed in section 2.4, a power system operator seeks to supply the reference values for \( P_2 \), \( Q_1 \), and \( Q_2 \). It is then the role of the HPFC controller to select an operating point for the converters and the shunt susceptance. The reachable set tables obtained as explained in section 3.4.2, may contain multiple operating points capable to meet the reference values for \( P_2 \), \( Q_1 \), and \( Q_2 \). Therefore, the controller must be capable of selecting a unique operating point.

In particular, there are five control variables (voltage vectors \( \vec{V}_X \) and \( \vec{V}_Y \) and the shunt susceptance \( B_M \)) yet only three reference values and one constraint equation. One degree of freedom therefore remains.

This gives rise to the notion of optimization. Suppose that each viable operating point can be assigned a scalar value representative of its “optimality”. For example, an operating point can be evaluated based on the total required converter kVA. The available degree of freedom can then be used to minimize the converter kVA.

In general, a selection of the operating point can be done in two steps.

1. All operating points that can meet the reference values for \( P_2 \), \( Q_1 \), and \( Q_2 \) are extracted from the reachable sets table, and recorded into another table.

2. An optimal operating point is extracted from the resulting table using a cost function analysis.
The first step can be implemented using a procedure represented by Algorithm B.1. The first part of Algorithm B.1 extracts those rows of reachable sets \textit{table} (described in section 3.4.2) that correspond to the given system voltages. The extracted rows are copied into \textit{table}$_1$. The second part of Algorithm B.1, analyzes the rows of \textit{table}$_1$, and extracts the ones containing $(P_{2\text{ref}}, Q_{1\text{ref}}, Q_{2\text{ref}})$, as follows. $P_{2\text{ref}}$ is first compared with $P_{2\text{min}}$ and $P_{2\text{max}}$ stored in the rows of \textit{table}$_1$. If $P_{2\text{ref}}$ lies between these values, then there exist $\overline{I}_S$ and $\overline{I}_R$ that result in a power flow exactly equal to $P_{2\text{ref}}$. The positions of $\overline{I}_S$ and $\overline{I}_R$ on their respective solution segments are proportional to the position of $P_{2\text{ref}}$ on the segment defined by $P_{2\text{min}}$ and $P_{2\text{max}}$. Once $\overline{I}_S$ and $\overline{I}_R$ are obtained, $Q_1$ and $Q_2$ are calculated. If they are near $Q_{1\text{ref}}$ and $Q_{2\text{ref}}$, respectively, the row of \textit{table}$_1$ is augmented with $\overline{I}_S$ and $\overline{I}_R$ and stored into \textit{table}$_2$.

An optimal operating point can then be extracted from rows of \textit{table}$_2$ by performing a cost function analysis. An implementation example of this analysis is illustrated by Algorithm B.2.

Together, the two algorithms can be viewed as a mapping from a triplet of scalar values $(P_2, Q_1, Q_2)$ to a quadruplet $(P_2, V_{Md}, V_{Mq}, B_M)$. This mapping is a solution for the problem of nonlinear constrained optimization, as identified in section 2.4.1.

It can be observed that the selected operating point will not be accurate due to the limited grid density and the neglected system losses. If desired, these inaccuracies can be further reduced by using numerical iterations. The setup for an iterative technique is greatly simplified, as it is not anymore necessary to consider the equipment limits or optimization. These considerations are accounted for by the selection of the initial point.

Alternatively, for real time controller implementation, the above inaccuracies can be ignored, and the convergence to the final operating point can be entrusted to the feedback loops of the controller. The controller structure proposed in Chapter 5 achieves the zero steady state error for $P_2$ and $Q_2$. The above inaccuracies therefore result in small static error of $Q_1$ and in a somewhat suboptimal “internal operating point” of the HPFC. In other words, by selecting the “rounded off” values for $B_M$ and $\overline{V}_M$, the converters may be forced to operate with slightly higher than optimal voltage magnitudes.
Algorithm B.1 Extract all rows of \( \text{table} \) that contain \((P_{2\text{ref}}, Q_{1\text{ref}}, Q_{2\text{ref}})\)

% Supply the reference values for \((P_2, Q_1, Q_2)\), and the tolerance:

\textbf{Input} : \(P_{2\text{ref}}, Q_{1\text{ref}}, Q_{2\text{ref}}, \text{tol}\)

\textbf{Input} : \(\text{table}\) % Load the reachable sets table

Supply the values of circuit parameters \(\to k, X_L\)

Supply the values of system voltages \(\to V_S, V_R, \delta\)

% Extract the rows of \(\text{table}\) that are nearest to \(V_S, V_R, \delta\), as follows:

\(\text{table}_1 \leftarrow \emptyset\) % Create an empty table

\textbf{for} row=1 to NumberOfRows(\(\text{table}\)) \textbf{do}

\hspace{1em}if \(\left| V_S - V_S(\text{row}) \right| \leq \text{tol} \&\& \left| V_R - V_R(\text{row}) \right| \leq \text{tol} \&\& \left| \delta - \delta(\text{row}) \right| \leq \text{tol}\) then

\hspace{2em}\(\text{table}_1 \leftarrow \text{AddRow}(\text{table}(\text{row}))\)

\hspace{1em}end if

\textbf{end for}

% Consider the rows of \(\text{table}_1\) and find those that contain \((P_{2\text{ref}}, Q_{1\text{ref}}, Q_{2\text{ref}})\), as follows:

\(\text{table}_2 \leftarrow \emptyset\) % Create an empty table

\textbf{for} row=1 to NumberOfRows(\(\text{table}_1\)) \textbf{do}

\hspace{1em}if \(P_{2\text{min}}(\text{row}) \leq P_{2\text{ref}} \leq P_{2\text{max}}(\text{row})\) then

\hspace{2em}\% \(P_{2\text{ref}}\) can be met, find exact \(\bar{I}_S\) and \(\bar{I}_R\) corresponding to \(P_{2\text{ref}}\), as follows:

\hspace{3em}\(\xi \leftarrow \frac{P_{2\text{ref}} - P_{2\text{min}}(\text{row})}{P_{2\text{max}}(\text{row}) - P_{2\text{min}}(\text{row})}\)

\hspace{3em}\(\bar{I}_S \leftarrow \xi(\bar{I}_{S_{\text{max}}}(\text{row}) - \bar{I}_{S_{\text{min}}}(\text{row})) + \bar{I}_{S_{\text{min}}}(\text{row})\)

\hspace{3em}\(\bar{I}_R \leftarrow \xi(\bar{I}_{R_{\text{max}}}(\text{row}) - \bar{I}_{R_{\text{min}}}(\text{row})) + \bar{I}_{R_{\text{min}}}(\text{row})\)

\hspace{2em}Compute \(Q_1\) and \(Q_2\) based on \(\bar{I}_S\) and \(\bar{I}_R\) \(\to Q_1, Q_2\)

\hspace{3em}if \(|Q_1 - Q_{1\text{ref}}| \leq \text{tol} \&\& |Q_2 - Q_{2\text{ref}}| \leq \text{tol}\) then

\hspace{4em}\% The solution point that meets \(P_{2\text{ref}},\) is also tolerably close to \(Q_{1\text{ref}}\) and \(Q_{2\text{ref}}\)

\hspace{5em}\(\text{table}_2 \leftarrow \text{AddRow}(\left[\text{table}_1(\text{row}), \bar{I}_S, \bar{I}_R\right])\)

\hspace{4em}end if

\hspace{2em}end if

\textbf{end for}

\textbf{Return} : \(\text{table}_2\)
Algorithm B.2 Choose the optimal operating point from table 2

% “CostFunction” is a scalar function whose minimum corresponds to the optimum

**Input**: table 2 % Each row of table 2 contains the solutions for \((P_{2\text{ref}}, Q_{1\text{ref}}, Q_{2\text{ref}})\)

Supply the values of circuit parameters \(\rightarrow k, X_L\)

% Calculate cost for each row of table 2 and store it into an array, as follows:

array \leftarrow \{\} % Create an empty array

for row=1 to NumberOfRows(table 2) do

\hspace{1em} cost \leftarrow \text{CostFunction}(table 2(row))

\hspace{1em} array \leftarrow \text{AddElement}(cost)

end for

Find the index of the minimal element of array \(\rightarrow \text{min}\)

**Return**: \(\bar{V}_M(\text{min}), B_M(\text{min}), \ldots\)
Appendix C

Current Controller Stability Analysis Relative to Errors in Estimates of Line Parameters
Defining frequency for convenience

\[ f := 60 \quad \omega := 2 \pi f \]

Defining the representative line parameters

\[ x_R := 0.462 \quad r_R := 0.022 \]

Defining the controller constants:

\[ kp := 0.2860 \quad T := 0.1457 \]

System matrix below has been derived based on Figure 5.5. Note that \( K_{VSC} K_M = Z_B \), i.e. the base impedance. Therefore, \( x_R (K_{VSC} K_M) = x_{Raccurate} \) and \( r_R (K_{VSC} K_M) = r_{Raccurate} \). Terms \( \Delta r_R \) and \( \Delta x_R \) are the relative errors of \( r_R \) and \( x_R \), respectively; e.g. \( \Delta x_R = (x_R - x_{Raccurate}) / x_{Raccurate} \).

Defining the system matrix dependent on error terms:

\[
A(\Delta r_R, \Delta x_R) := \begin{pmatrix}
\omega \frac{\Delta r_R}{x_R} & -\frac{\omega}{x_R} kp & \omega \frac{\Delta x_R}{x_R} & \omega \\
\frac{1}{r_R} & 0 & 0 & 0 \\
-\omega \frac{\Delta x_R}{x_R} & \omega \frac{\Delta r_R}{x_R} & -\frac{\omega}{x_R} kp & 0 \\
\frac{1}{T} & 0 & 0 & 0 \\
0 & \frac{1}{T} & 0 & 0
\end{pmatrix}
\]

\[
eigvals(A(0, 0)) = \begin{pmatrix}
-206.217 \\
-27.158 \\
-206.217 \\
-27.158
\end{pmatrix} \quad \text{eigvals}(A(0.2, 0.2)) = \begin{pmatrix}
-206.595 + 84.931i \\
-206.595 - 84.931i \\
-23.19 + 9.533i \\
-23.19 - 9.533i
\end{pmatrix}
\]

\[
eigvals(A(-0.2, -0.2)) = \begin{pmatrix}
-214.337 + 84.298i \\
-214.337 - 84.298i \\
-22.629 + 8.9i \\
-22.629 - 8.9i
\end{pmatrix}
\]
Introducing the term "m" to quantify the error.
The term "m" is defined as \( x_{\text{model}} = m \times x_{\text{actual}} \)

Varying the estimate of reactance:
\[
\begin{align*}
c(m) &:= \text{eigenvals}(A_0(m - 1)) \quad m := 0.1, 0.11..2 
\end{align*}
\]
\[
c(1) \text{ represents the accurate value:}
\[
\begin{pmatrix}
  -206.217 \\
  -27.158 \\
  -206.217 \\
  -27.158
\end{pmatrix}
\]

Figure C.2: Page 2 – Root locus for error in estimate of line reactance
Varying the estimate of resistance:

c(m) := eigenvals(A(m - 1, 0)) \quad m := 0.1, 0.11..2

Figure C.3: Page 3 – Root locus for error in estimate of line resistance
Varying the estimates of reactance and resistance simultaneously (maintaining X/R constant):

\[ c(m) := \text{eigvals}(A(m - 1, m - 1)) \quad m := 0.01, 0.02, 2 \]

\[
\begin{align*}
\text{c}(0) &= \begin{pmatrix}
-244.797 + 387.323i \\
-244.797 - 387.323i \\
-6.53 + 10.332i \\
-6.53 - 10.332i
\end{pmatrix} \\
\text{c}(1) &= \begin{pmatrix}
-206.217 \\
-27.158 \\
-206.217 \\
-27.158
\end{pmatrix} \\
\text{c}(2) &= \begin{pmatrix}
-209.395 + 388.167i \\
-209.395 - 388.167i \\
-6.029 + 11.176i \\
-6.029 - 11.176i
\end{pmatrix}
\]

Figure C.4: Page 4 – Root locus for simultaneous error in estimate of line reactance and resistance (X/R=const)
APPENDIX C. CURRENT CONTROLLER STABILITY ANALYSIS

Tabulated values for range of error -/+20% (simultaneous variation of resistance and reactance):

\[ m := 0.8, 0.85..1.2 \]

<table>
<thead>
<tr>
<th>( c(m)_0 )</th>
<th>( c(m)_1 )</th>
<th>( c(m)_2 )</th>
<th>( c(m)_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>-214.337+84.298i</td>
<td>-214.337-84.298i</td>
<td>-22.629+8.9i</td>
<td>-22.629-8.9i</td>
</tr>
<tr>
<td>-211.832+63.854i</td>
<td>-211.832-63.854i</td>
<td>-24.236+7.306i</td>
<td>-24.236-7.306i</td>
</tr>
<tr>
<td>-209.519+42.959i</td>
<td>-209.519-42.959i</td>
<td>-25.652+5.26i</td>
<td>-25.652-5.26i</td>
</tr>
<tr>
<td>-207.583+21.631i</td>
<td>-207.583-21.631i</td>
<td>-26.69+2.781i</td>
<td>-26.69-2.781i</td>
</tr>
<tr>
<td>-205.477+43.185i</td>
<td>-205.477-43.185i</td>
<td>-26.103+5.486i</td>
<td>-26.103-5.486i</td>
</tr>
<tr>
<td>-205.898+64.287i</td>
<td>-205.898-64.287i</td>
<td>-24.784+7.738i</td>
<td>-24.784-7.738i</td>
</tr>
<tr>
<td>-206.595+84.931i</td>
<td>-206.595-84.931i</td>
<td>-23.19+9.533i</td>
<td>-23.19-9.533i</td>
</tr>
</tbody>
</table>

Tabulated values for range of error -/+100% (simultaneous variation of resistance and reactance):

\[ m := 0, 0.1..2 \]

<table>
<thead>
<tr>
<th>( c(m)_0 )</th>
<th>( c(m)_1 )</th>
<th>( c(m)_2 )</th>
<th>( c(m)_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>-244.797+387.323i</td>
<td>-244.797-387.323i</td>
<td>-6.53+10.332i</td>
<td>-6.53-10.332i</td>
</tr>
<tr>
<td>-242.05+350.115i</td>
<td>-242.05-350.115i</td>
<td>-7.483+10.823i</td>
<td>-7.483-10.823i</td>
</tr>
<tr>
<td>-239.102+312.893i</td>
<td>-239.102-312.893i</td>
<td>-8.635+11.3i</td>
<td>-8.635-11.3i</td>
</tr>
<tr>
<td>-235.904+275.622i</td>
<td>-235.904-275.622i</td>
<td>-10.038+11.728i</td>
<td>-10.038-11.728i</td>
</tr>
<tr>
<td>-232.396+238.24i</td>
<td>-232.396-238.24i</td>
<td>-11.75+12.046i</td>
<td>-11.75-12.046i</td>
</tr>
<tr>
<td>-224.191+162.671i</td>
<td>-224.191-162.671i</td>
<td>-16.365+11.874i</td>
<td>-16.365-11.874i</td>
</tr>
<tr>
<td>-214.337+84.298i</td>
<td>-214.337-84.298i</td>
<td>-22.629+8.9i</td>
<td>-22.629-8.9i</td>
</tr>
<tr>
<td>-209.519+42.959i</td>
<td>-209.519-42.959i</td>
<td>-25.652+5.26i</td>
<td>-25.652-5.26i</td>
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<tr>
<td>-205.477+43.185i</td>
<td>-205.477-43.185i</td>
<td>-26.103+5.486i</td>
<td>-26.103-5.486i</td>
</tr>
<tr>
<td>-205.898+64.287i</td>
<td>-205.898-64.287i</td>
<td>-24.784+7.738i</td>
<td>-24.784-7.738i</td>
</tr>
<tr>
<td>-206.595+84.931i</td>
<td>-206.595-84.931i</td>
<td>-23.19+9.533i</td>
<td>-23.19-9.533i</td>
</tr>
</tbody>
</table>

Figure C.5: Page 5 – Tabulated root values for simultaneous error in estimate of line reactance and resistance (X/R=const)
Appendix D

The PSCAD Model
Notice the phasing of VSCY and the connection of secondaries to the transmission line; it holds that: 

\[ VM + VY = V2 \]
Figure D.3: Plots
Figure D.4: Plots_2
DC Capacitor's dynamics are modelled in this sheet. Since the converters are represented as voltage sources, it is not possible to use electrical circuit for simulation of DC caps.

Charging current is derived based on active power drawn by the two VSCs. The voltage (charge) on the capacitor is then calculated by integration of the charging current.

With caps at rated voltage, and both converters operated to supply their rated MVA to charge the caps, the charging rate is to result in full charge during one cycle of line frequency. That is:

\[ \text{C} = \frac{\text{MVA}}{\text{V}} \times \frac{1}{2} \times \frac{1}{f} \]

Hence:

\[ \text{C} = \frac{4\, \text{MVA}}{\text{V}} \times \frac{1}{2} \times \frac{1}{f} \times \frac{1}{1.67} \approx \frac{0.4446 \, \text{F}}{\text{C}} \]

or to make it a round number \( \text{C} = 0.5 \, \text{F} \)

Gain factor before the integrator is 1/C, that is 2.0

Incoming voltage signals, as well as voltage on dc caps are in [kV]. Incoming current signal is in [kA]. Computed signal \( I_{DC} \) is in kA.
Figure D.6: SCR Controlled Inductor Bank (12 Pulse)
**APPENDIX D. THE PSCAD MODEL**

**Figure D.7: SCR Switched capacitors (typical)**

When enable signal exists, the SCRs are fired. Firing signals are generated inside the block and take into account the charge on the caps.
For derivation of this see: \texttt{hpfc_bm.mod}

\begin{verbatim}
hpfc_800 -> SVC_Control                     firing angle for inductor bank and enable signals for cap banks are generated
\end{verbatim}

\textbf{Figure D.8: SVC control}
APPENDIX D. THE PSCAD MODEL

\[
\begin{align*}
G_1 + sT
\end{align*}
\]

\[
\begin{align*}
V_{1c} & \quad V_{1b} \quad V_{1d} \\
V_{1q} & \quad V_{1a} \quad \theta_1
\end{align*}
\]

\[
\begin{align*}
V_{2d} & \quad V_{2q} \quad V_{2a} \quad \theta
\end{align*}
\]

\[
\begin{align*}
IS_d & \quad IS_q \quad IS_a \quad IS_b
\end{align*}
\]

\[
\begin{align*}
V_{Sd} & \quad VM_d \quad VM_q \\
V_{Sc} & \quad VS_q \quad VR_d
\end{align*}
\]

\[
\begin{align*}
VR_a & \quad VR_b \quad VR_c \quad VR_q
\end{align*}
\]

\[
\begin{align*}
V_{IRd} & \quad IS_{dq} \quad VS_{dq}
\end{align*}
\]

\[
\begin{align*}
IS_{dq} & \quad VS_{dq}
\end{align*}
\]

\[
\begin{align*}
IM_{dq} & \quad IM_{dq}
\end{align*}
\]

\[
\begin{align*}
IM_a & \quad IM_b
\end{align*}
\]

\[
\begin{align*}
1/I_b, \text{ where } I_b = 1.5 \text{kA} \\
\text{incoming signal already in kA}
\end{align*}
\]

\[
\begin{align*}
1/V_b, \text{ where } V_b = 13kV/\text{sqrt}(3) \\
\text{incoming signal already in kV}
\end{align*}
\]

\[
\begin{align*}
1/V_b, \text{ where } V_b = 230kV/\text{sqrt}(3) \\
\text{incoming signal already in kV}
\end{align*}
\]

\[
\begin{align*}
\phi_{corr} \quad \phi_{in} \quad \phi_{out}
\end{align*}
\]

\[
\begin{align*}
\text{Phase Correction}
\end{align*}
\]
Figure D.11: Phase correction for abc2dq transformation
Figure D.12: V S estimation and power measurements
Figure D.13: Current regulator – overview
Figure D.14: Current regulator ($\psi_n < 0$)
Figure D.15: Current regulator ($\phi_n = 0$)
Figure D.16: Current regulator ($\gamma_1 > 0$)
Figure D.17: Current reference computer – overview
Figure D.18: Current reference computer ($\beta > 0$)
Figure D.19: Current reference computer ($n = 0$)
Figure D.20: Current reference computer ($bM < 0$)
Figure D.21: dq2abc transformation

VSC angle is phase shifted to account for the transformer connection
See notes Feb 19-20/02

Outputs are applied only when the regulator is enabled

G=1, z=0.5, f=200Hz

V_Xd 1 + \frac{2z}{s} - \frac{Wo^2}{s^2} V_Yd

V_Xq 1 + 2zWo s - Wo^2 V_Yq

Move these signals after the filters when working with bM=0

En

See notes Mar 29/02 @3:15PM